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GPI65007DF88

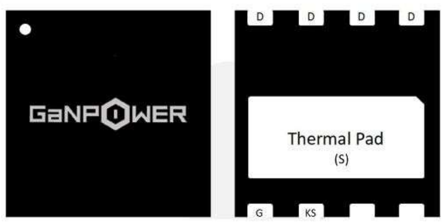
N-channel 650V 7A GaN Power HEMT in DFN 8X8 Package

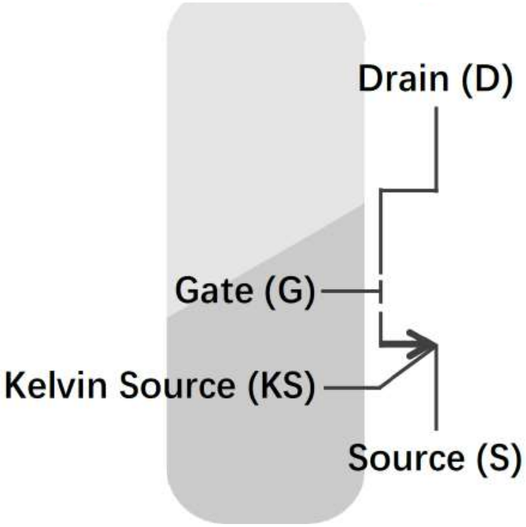
Datasheet version 2.5 Preliminary

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g
650 V	170 mΩ	7 A	2.1 nC

- Ultra-low R_{DS}(on)
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile





Applications

- Switching Power Applications
- Adapters, Quick Chargers

Description

These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

Device Characteristics

Static Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$, $I_d=3.5$ mA ($T_J=25$ °C)	1.0	1.2	1.5	V
			$V_{ds}=V_{gs}$, $I_d=3.5$mA ($T_J=150$ °C)		1.15		V
2	BV_{dss}	Drain-Source breakdown voltage	$V_{gs}=0$V, $I_d < 1$ μA ($T_J=25$ °C)		650		V
3	I_{dss}	Zero gate voltage drain leakage current	$V_{gs}=0$V, $V_{ds}=650$V $T_J=25$ ℃		0.1	1	μA
4	I_{gss}	Gate-Source Leakage	$V_{gs}=6$V, $V_{ds}=0$V		5	80	μA
5	R_{dson}	drain-source on resistance	$V_{gs}=6$V, $I_d=2.5$A $T_J=25$ ℃		170	230	mΩ
			$V_{gs}=6$V, $I_d=2.5$A $T_J=150$ ℃		420		mΩ
6	V_{sd}	Reverse conduction voltage	$I_{sd}=1$A, $V_{gs}=0$V	1.4	2.2	3	V
7	R_g	Gate resistance	f=25Mhz Open drain		1.1		Ω
Dynamic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{ISS}	Input capacitance	$V_{gs}=0$ V $V_{ds}=500$ V f = 100 kHz		60		pf
2	C_{OSS}	Output capacitance			16		pf
3	C_{RSS}	Reverse transfer capacitance			0.37		pf
4	CO(er)	Effective output capacitance, energy related	Vds = 0 - 500V		22.7		pf
5	Q_g	Gate charge	Vds = 500V Id = 1.75A Vgs = 6V		2.1		nC
6	Q_{gs}	Gate to source charge			0.4		nC
7	Q_{gd}	Gate to drain charge			0.52		nC
8	QOSS	Output Charge	Vds = 0 - 500V		18		nC
9	Q_{rr}	Reverse recovery charge			0		nC

Switching Performance				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$t_{d(on)}$	Turn-on delay time	V_{ds} = 500V I_d = 1.75A R_g = 10Ω V_{gs} = 6V		4		ns
2	t_r	Rise time			8		ns
3	$t_{d(off)}$	Turn-off delay time			14		ns
4	t_f	Fall time			8		ns

Absolute Max. Ratings

	Symbols	**Parameters**	**Value**	**Unit**
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=25°C	800	V
2	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=125°C	650	V
3	$V_{GS\text{-}max}$	Gate to source max. voltage @ T_{case}=25°C	-12 to +7.5	V
4	$I_{ds\text{-}max}$	Drain to source pulse current @ T_{case}=25°C, pulse width 10 μs, V_{GS} = 6 V	16	A
5	$I_{ds\text{-}max}$	Drain to source pulse current @ T_{case}=150°C	7	A
6	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	200	V/ns
7	$T_{J\text{-}max}$	Max junction temperature	150	°C
8	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

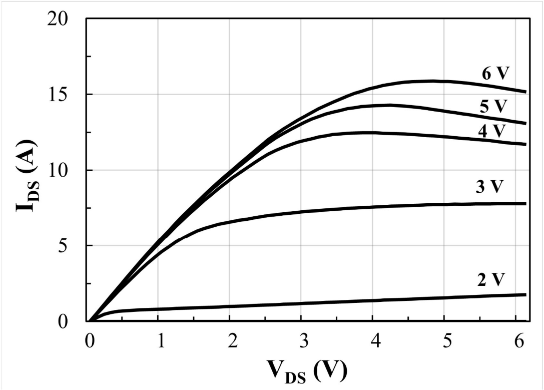
Thermal and Soldering Characteristics (Typical)

	Symbols	**Parameters**	**Value**	**Unit**
1	R_{thJC}	Thermal resistance (junction to case)	2.2	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	250	°C

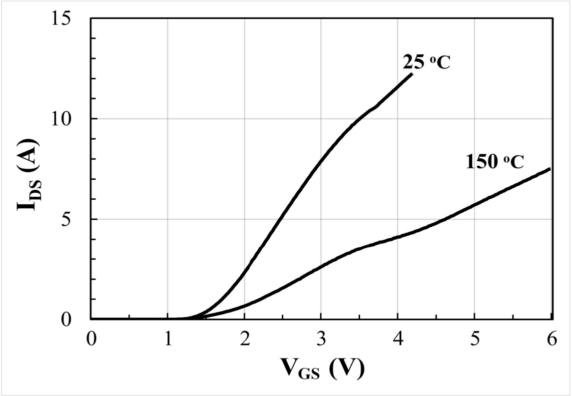
Ordering

Order Code	**Package Type**	**Packaging Method**	**Qty**
GPI65007DF88	DFN surface mount, bottom cooled, 8X8 mm		

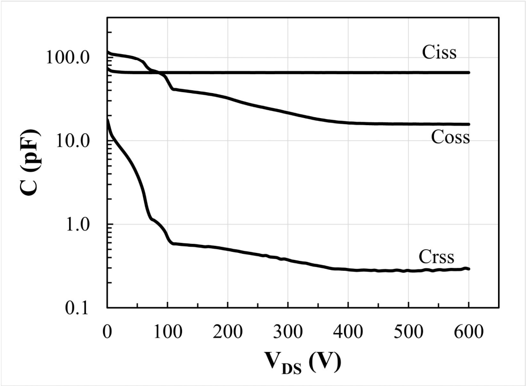
Electrical Performance



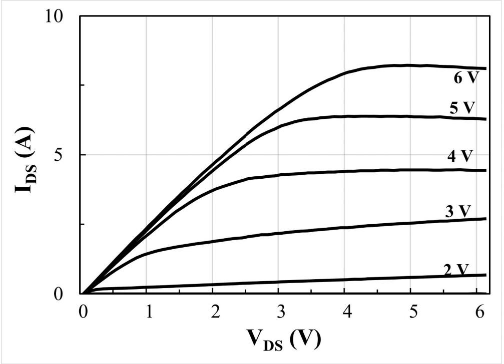
I_{DS} vs. V_{DS} @ T_j = 25 °C



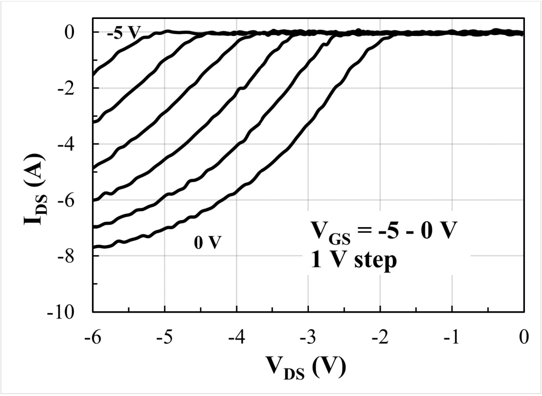
I_{DS} vs. V_{GS} @ T_j = 25 °C and 150 °C



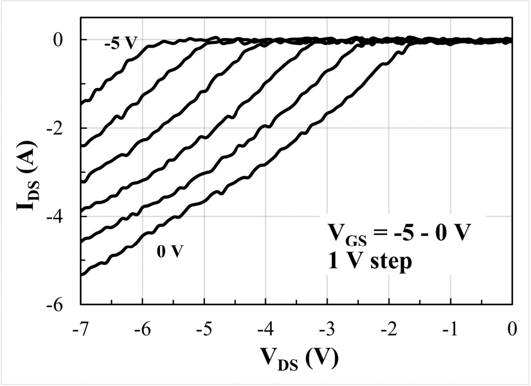
Capacitance vs. V_{ds} Curve @ T_j =25 °C



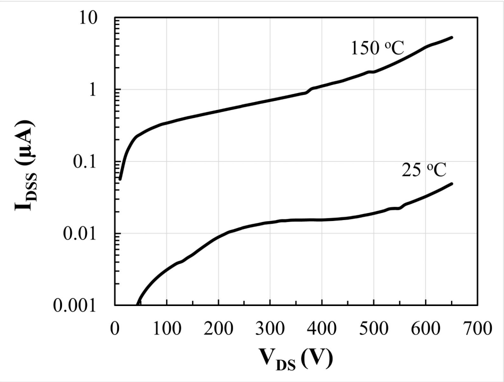
I_{DS} vs. V_{DS} @ T_j = 150 °C



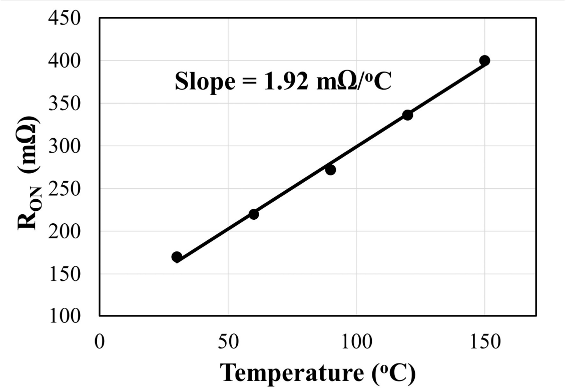
I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 25 °C



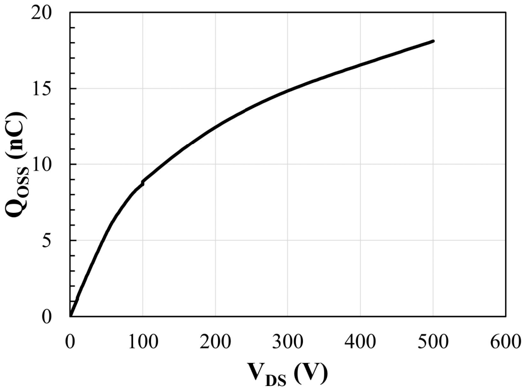
I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 150°C



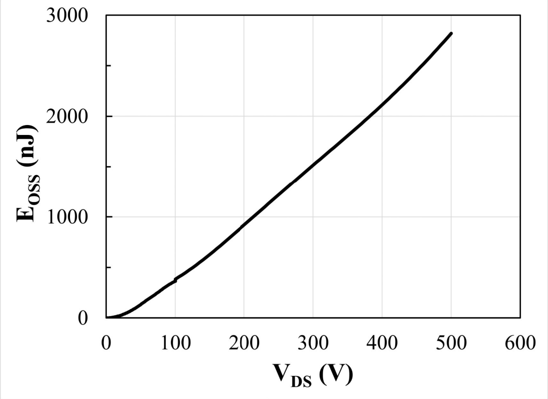
Typical off-state drain leakage current I_{DSS} vs. V_{DS} @ T_J = 25 °C and 150 °C



On-state resistance vs. T_J @ I_D = 1.75 A, V_{GS} = 6V

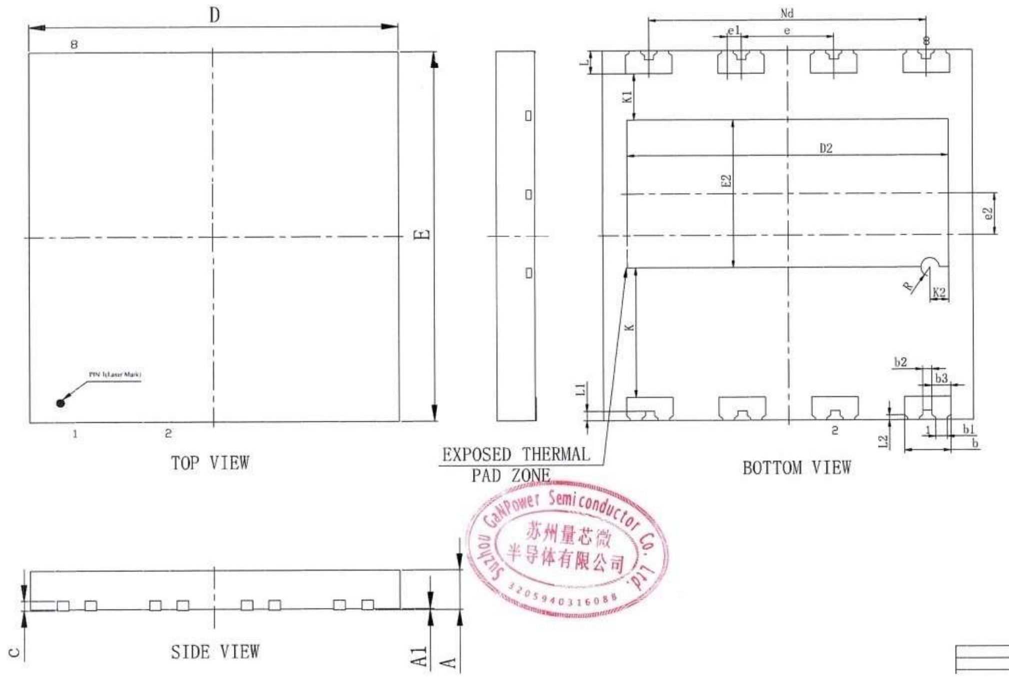


Output charge Q_{OSS} vs. V_{DS}



Stored Energy Characteristic E_{OSS} vs. V_{DS}

Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.95	1.00	1.05
b1	0.25REF		
b2	0.20REF		
b3	0.35	0.40	0.45
c	0.203REF		
D	7.90	8.00	8.10
D2	6.84	6.94	7.04
Nd	6.00BSC		
e	2.00BSC		
e1	0.30BSC		
e2	0.90BSC		
E	7.90	8.00	8.10
E2	3.10	3.20	3.30
L	0.45	0.50	0.55
L1	0.20REF		
L2	0.10REF		
K	2.80REF		
K1	1.00REF		
K2	0.40REF		
R	0.15	0.20	0.25

GaN HEMT Frequently Asked Questions

1	Q: Can we do pin to pin switch for silicon MOSFET or IGBT? A: The short answer is no. GaN HEMT power devices are far superior than the best silicon devices such as super junction MOSFETs. However, due to different requirements of gate driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layouts are recommended to minimize the impact from circuit parasitics.
2	Q: How do GaN power devices compare with SiC? A: Currently GaN power HEMT devices are most suitable for low to medium voltage (⩽1200V) and power (<20KW) applications. GaN is the ideal choice for high frequency applications. SiC devices are better choice for high voltage and high-power applications (>20KW).
3	Q: Do we need to parallel an FRD for applications such as inverters? A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent PN junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for the purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operate in both first and third quadrants. However, care should be taken for the dead time power loss since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative gate voltage is applied.
4	Q: Can we parallel GaN HEMT devices? A: Yes, GaN HEMT is ideal for paralleling, due to the positive temperature coefficient of $R_{ds,on}$. Hence, paralleling GaN HEMT devices are encouraged.