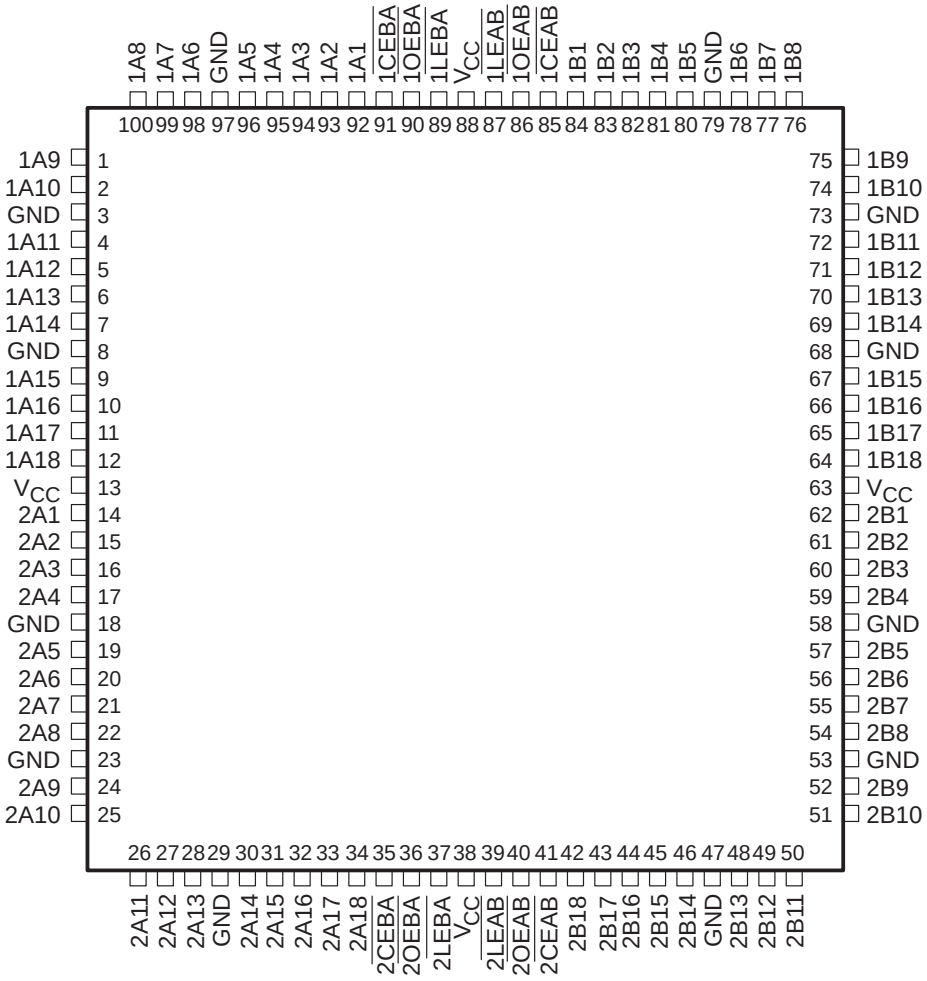
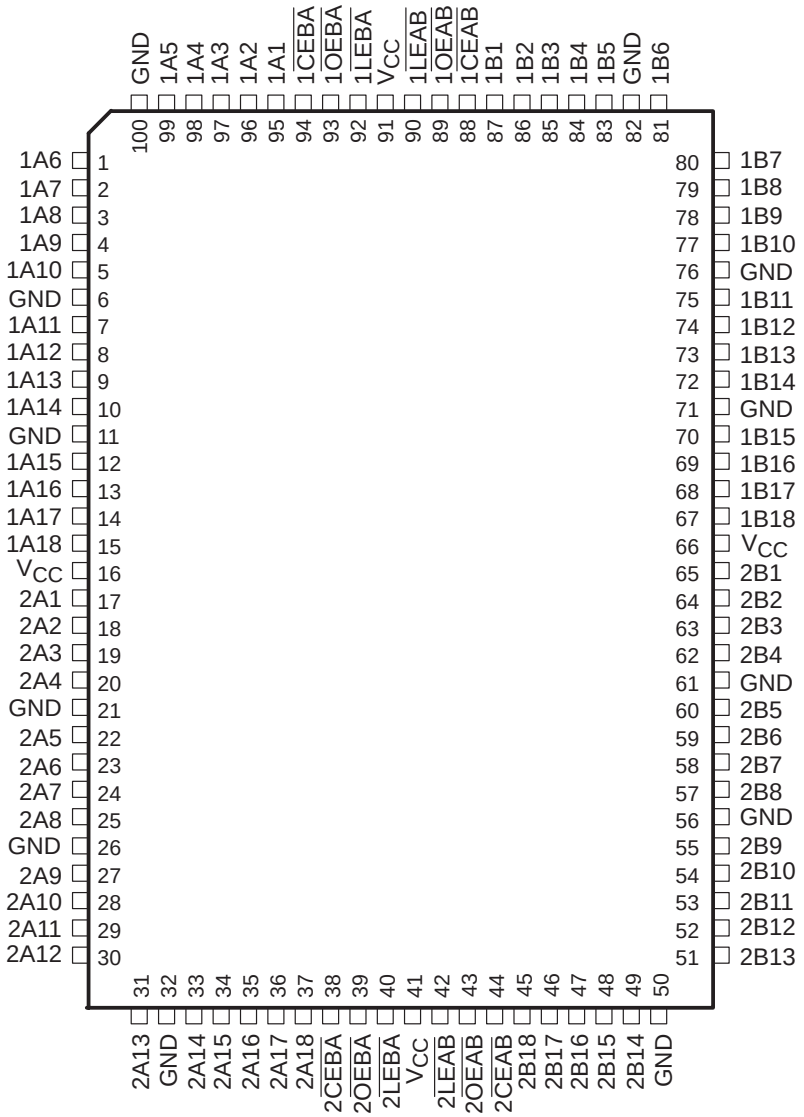
- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Released as DSCC SMD 5962-9557801NXD**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With 14 × 14-mm Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†**

'ABTH32543 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.

SN54ABTH32543 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The 'ABTH32543 are 36-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. These devices can be used as two 18-bit transceivers or one 36-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH32543 is characterized for operation from –40°C to 85°C.

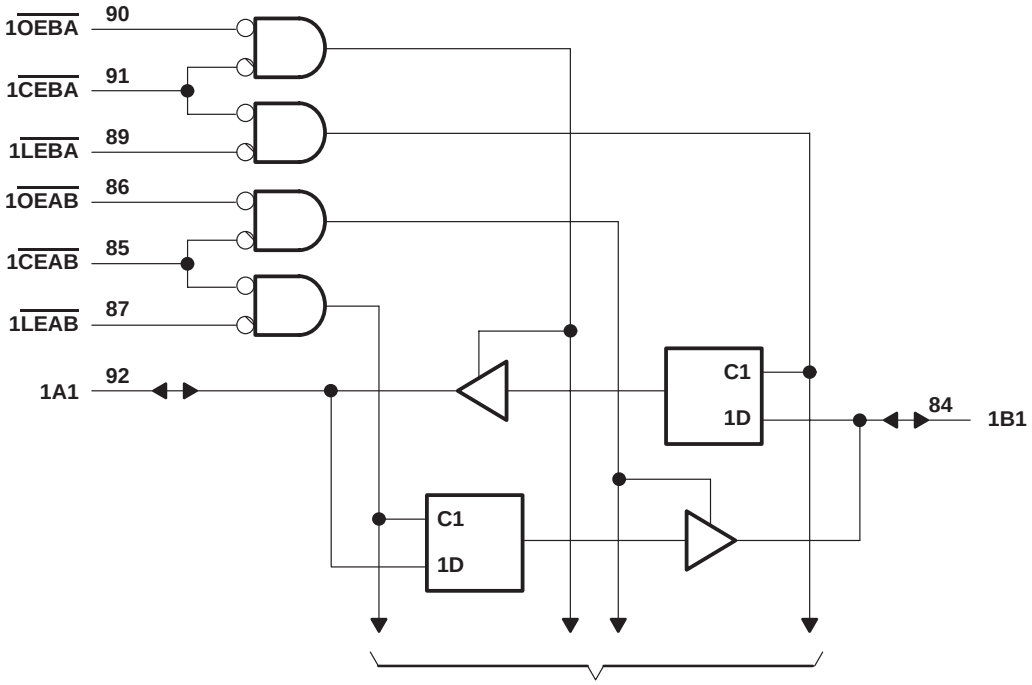
FUNCTION TABLE† (each 18-bit section)

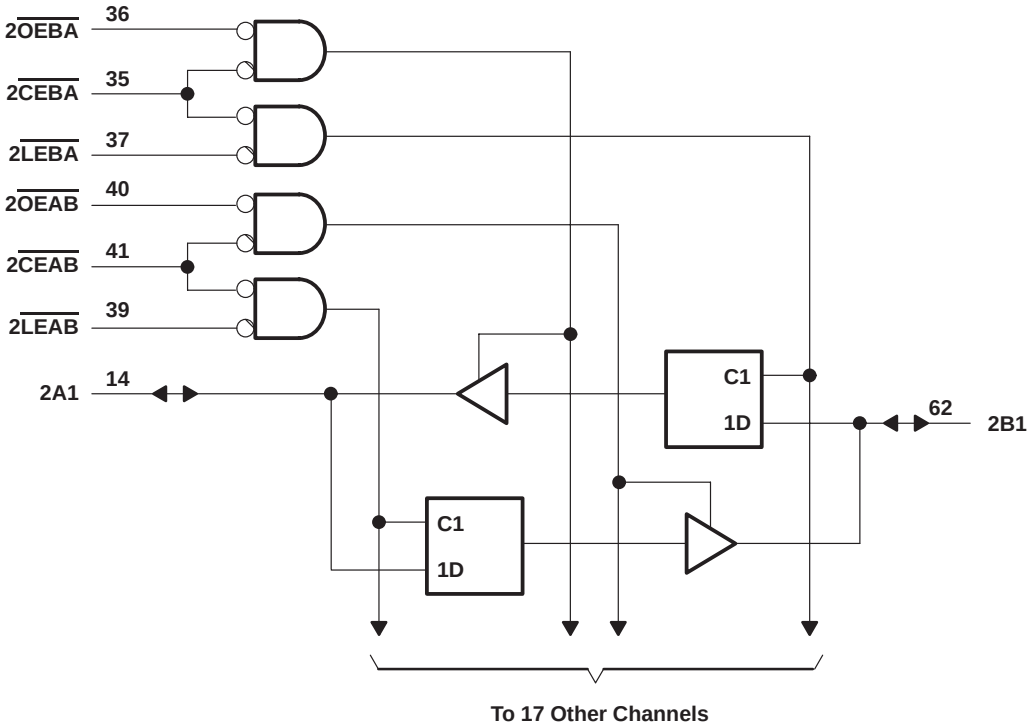
INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

‡ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)





Pin numbers shown are for the PZ package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABTH32543 . . . . . 96 mA
SN74ABTH32543 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package . . . . . 50°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTH32543			SN74ABTH32543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.5			2.5			V
		V_{CC} = 5 V,	I_{OH} = – 3 mA	3			3			
		V_{CC} = 4.5 V	I_{OH} = – 24 mA	2						
			I_{OH} = – 32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
V_{hys}					100			100		mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V,	V_I = V_{CC} or GND						±20	
	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1				
	A or B ports					±20				
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V				100			µA
			V_I = 2 V				–100			
I_{OZPU}‡		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{OZPD}‡		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3			3	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1			1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3.5			3.5		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9.5			9.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is specified by characterization.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C#		SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before $\overline{LEAB}$↑ or $\overline{LEBA}$↑	2.1		2.6		2.1		ns
		Data before $\overline{CEAB}$↑ or $\overline{CEBA}$↑	1.7		2		1.7		
t_h	Hold time	Data after $\overline{LEAB}$↑ or $\overline{LEBA}$↑	0.6		1.1		0.6		ns
		Data after $\overline{CEAB}$↑ or $\overline{CEBA}$↑	0.9		1.2		0.9		

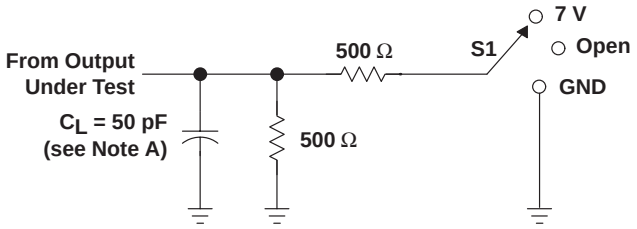
These limits apply only to the SN74ABTH32543.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C†			SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.2	0.5	6.3	1	5.9	ns
t_{PHL}			1	3.5	5.1	0.5	5.9	1	5.7	
t_{PLH}	$\overline{LE}$	A or B	1.9	4.6	6.3	0.8	7.9	1.9	7.5	ns
t_{PHL}			1.9	4.3	5.9	0.8	6.9	1.9	6.6	
t_{PZH}	$\overline{CE}$	A or B	1.7	4.3	6.7	0.8	8.3	1.7	8	ns
t_{PZL}			2.6	5.2	8	1	8.8	2.6	8.8	
t_{PHZ}	$\overline{CE}$	A or B	1.6	3.8	6.6	0.5	7.4	1.6	7.1	ns
t_{PLZ}			2.4	4.6	7	1	7.9	2.4	7.5	
t_{PZH}	$\overline{OE}$	A or B	1.4	3.8	6.1	0.5	7.6	1.4	7.3	ns
t_{PZL}			2.3	4.7	7.4	1	8.2	2.3	8.1	
t_{PHZ}	$\overline{OE}$	A or B	1.3	3.4	6.1	0.5	6.7	1.3	6.5	ns
t_{PLZ}			2	4.2	6.6	0.8	7.2	2	6.9	

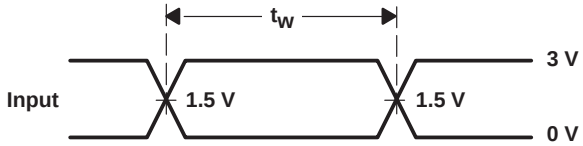
† These limits apply only to the SN74ABTH32543.

PARAMETER MEASUREMENT INFORMATION

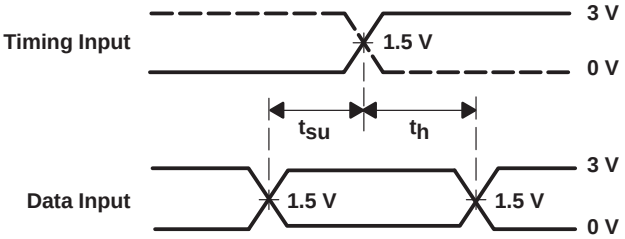


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

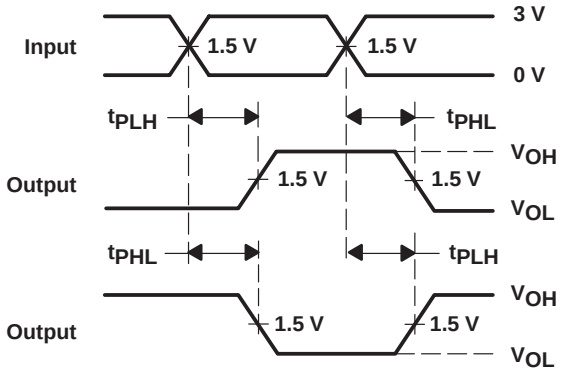
LOAD CIRCUIT



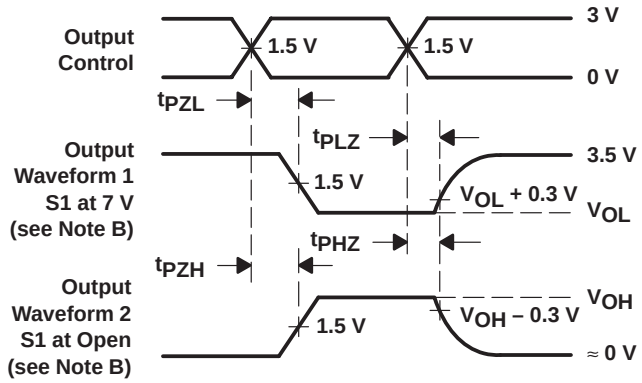
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9557801NXD	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	9557801NXD ABTH32543	Samples
SN74ABTH32543PZ	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32543	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

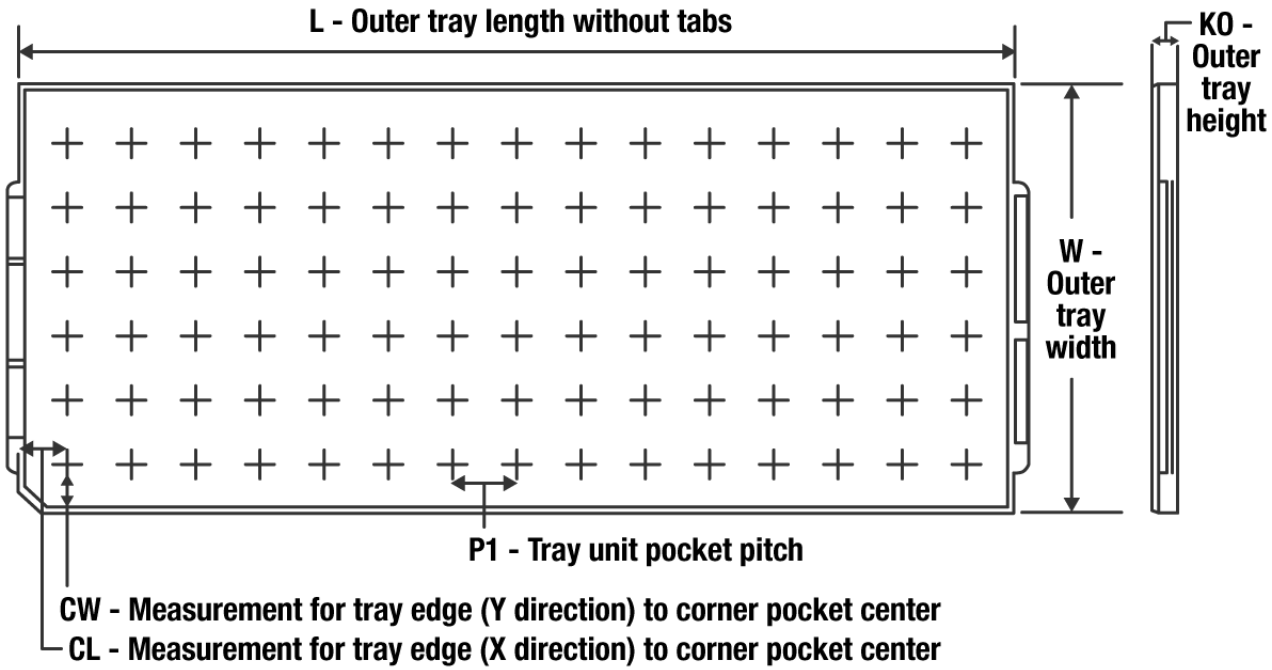
OTHER QUALIFIED VERSIONS OF SN54ABTH32543, SN74ABTH32543 :

- Catalog : SN74ABTH32543
- Military : SN54ABTH32543

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TRAY



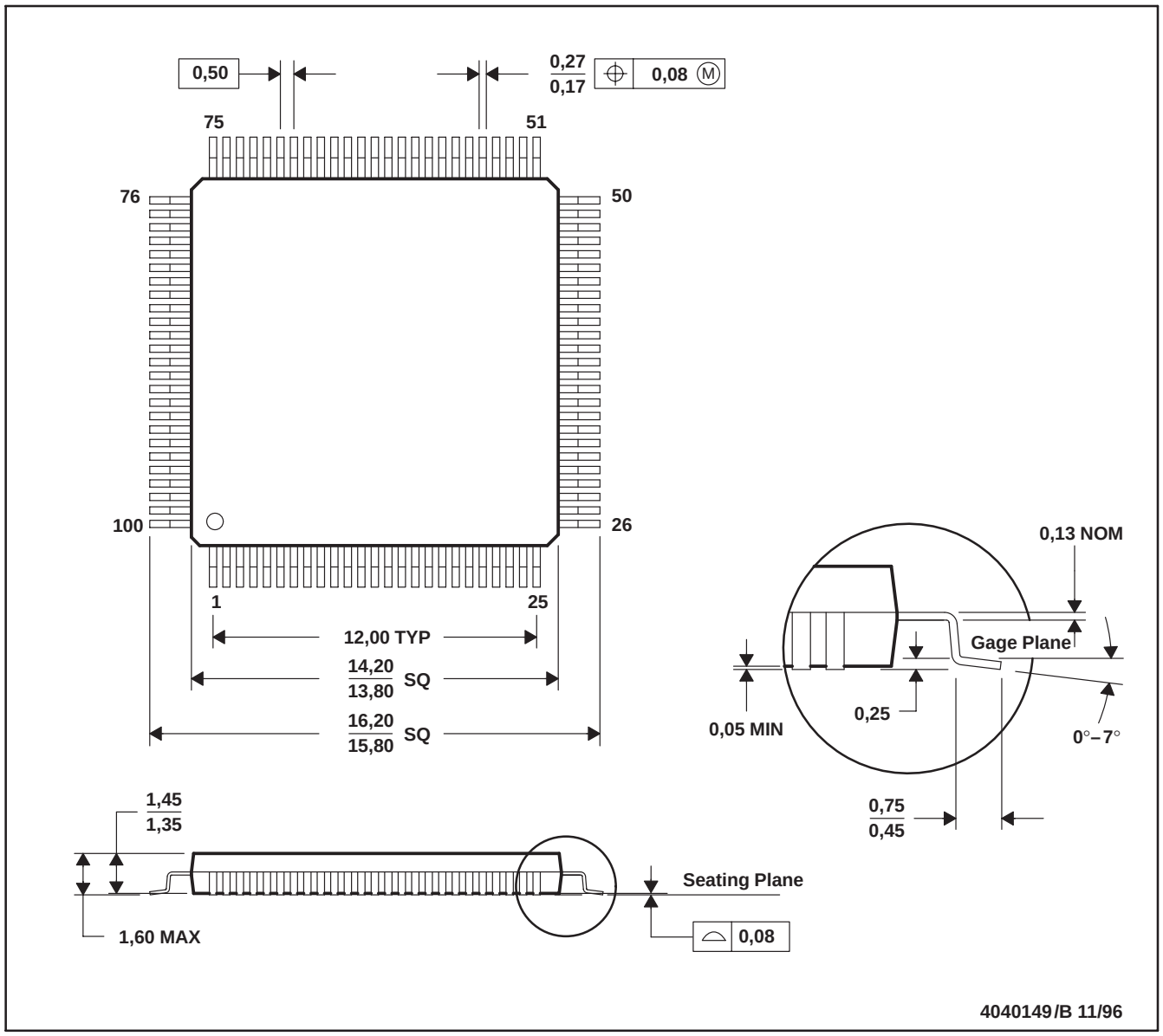
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9557801NXD	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74ABTH32543PZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

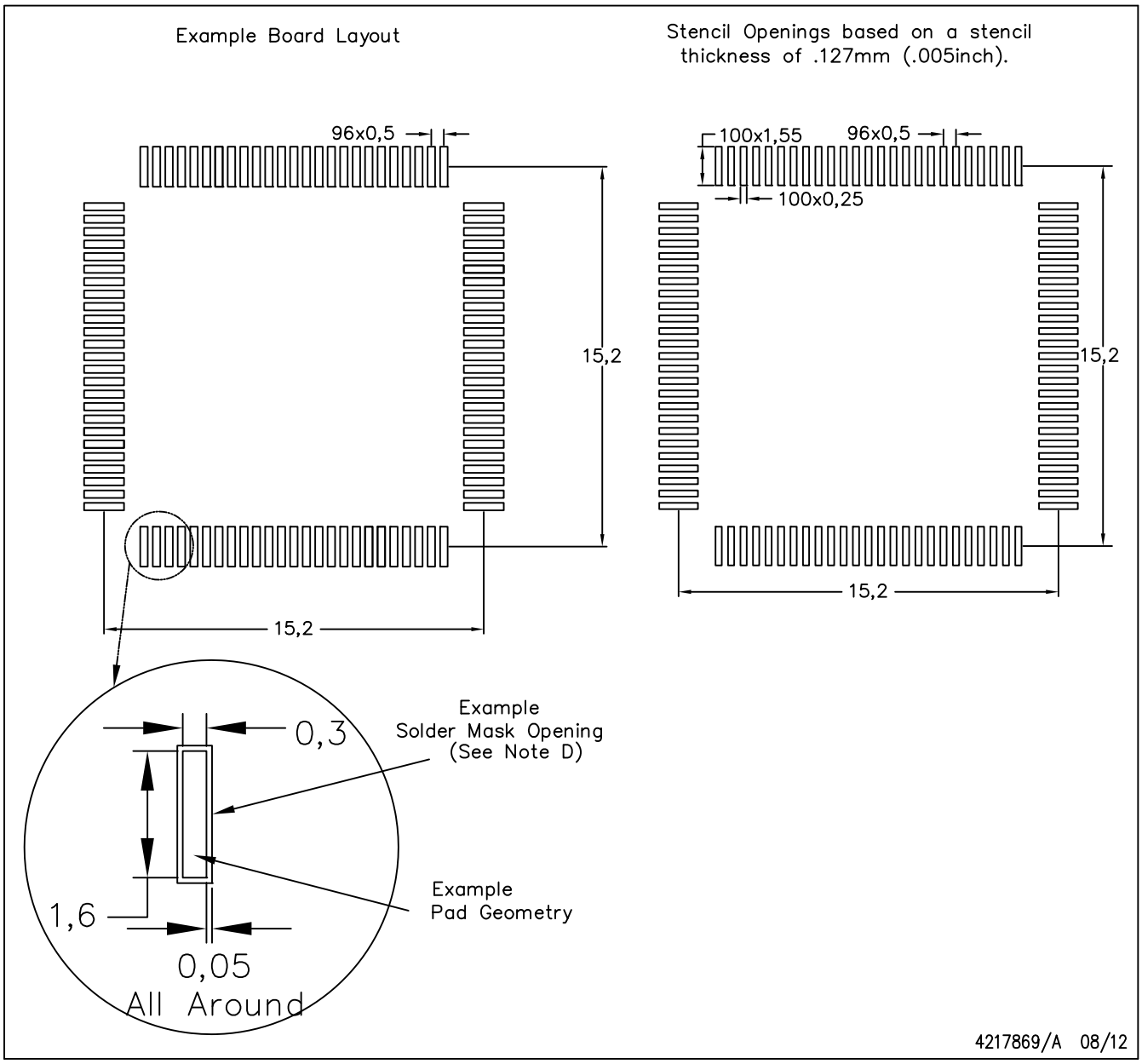
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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