MSP430FG662x, MSP430FG642x Mixed-Signal Microcontrollers

1 Features

- Low supply voltage range:
  3.6 V down to 1.8 V
- High-performance integrated signal chain
  - Continuous-time sigma-delta 16-bit analog-to-digital converter (ADC) with internal reference with 10 external analog inputs, 6 single-ended and 4 selectable as differential or single-ended
  - Dual operational amplifiers
  - Quad low-impedance ground switches
  - Voltage comparator
- Dual 12-bit digital-to-analog converters (DACs) with synchronization
- Integrated LCD driver with contrast control for up to 160 segments
- MSP430FG662x: Full-speed universal serial bus (USB)
  - Integrated USB-PHY
  - Integrated 3.3-V and 1.8-V USB power system
  - Integrated USB-PLL
  - Eight input and eight output endpoints
- Ultra-low power consumption
  - Active mode (AM),
    all system clocks active:
    250 µA/MHz at 8 MHz, 3.0 V, flash program execution (typical)
  - Standby mode (LPM3):
    watchdog with crystal, and supply supervisor operational, full RAM retention, fast wakeup:
    3.2 µA at 2.2 V, 3.4 µA at 3.0 V (typical)
  - Shutdown RTC mode (LPM3.5):
    shutdown mode, active RTC with crystal:
    0.9 µA at 3.0 V (typical)
  - Shutdown mode (LPM4.5):
    0.2 µA at 3.0 V (typical)
- Intelligent digital peripherals
  - Two 16-bit timers with three capture/compare registers each
  - One 16-bit timer with five capture/compare registers
  - One 16-bit timer with seven capture/compare registers
  - 6-channel internal DMA
  - Hardware multiplier supports 32-bit operations
- Four universal serial communication interfaces (USCIs)
  - USCI_A0 and USCI_A1
    - Enhanced UART with automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1
    - I^2C
    - Synchronous SPI
- RTC with calibration logic for time offset correction, operation in LPM 3.5
- 16-bit RISC architecture, extended memory, up to 20-MHz system clock
- Flexible power-management system
  - Fully integrated LDO with programmable regulated core supply voltage
  - Supply voltage supervision, monitoring, and brownout
- Unified clock system
  - FLL control loop for frequency stabilization
  - Low-power low-frequency internal clock source (VLO)
  - Low-frequency trimmed internal reference source (REFO)
  - 32-kHz crystals (XT1)
  - High-frequency crystals up to 32 MHz (XT2)
- Separate voltage supply for backup subsystem
  - 32-kHz low-frequency oscillator (XT1)
  - RTC
  - Backup memory (8 bytes)
- Development tools and software (also see Tools and Software)
  - MSP-TS430PZ100AUSB 100-pin target development board
  - MSP430Ware™ code examples
- Wake up from standby mode in 3 µs (typical)
- Serial onboard programming, no external programming voltage needed
- Available in 100-pin LQFP and 113-pin Microstar Junior™ BGA packages
- Device Comparison summarizes the available family members

2 Applications

- Analog sensor systems
- Digital sensor systems
- Hand-held meters
- Medical diagnostic meters
- Hand-held industrial testers
- Measurement equipment

3 Description

The Texas Instruments MSP430FG662x and MSP430FG642x microcontrollers (MCUs) are part of the MSP430TM Metrology and Monitoring portfolio. The architecture and integrated peripherals, combined with five extensive low-power modes, are optimized to achieve extended battery life in portable and battery-powered measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430FG662x MCUs are targeted at small signal-monitoring applications and include a 16-bit sigma-delta ADC, dual low-power operational amplifiers, dual 12-bit DACs, voltage comparator, four USCIs (two USCI_A modules and two USCI_B modules), four 16-bit timers, a hardware multiplier, a DMA module, an RTC module, an LCD driver with integrated contrast control for up to 160 segments, integrated full-speed USB, an auxiliary supply system, up to 128KB flash, 10KB SRAM and 73 I/O pins in 100-pin devices and 113-pin devices.

The MSP430FG642x MCUs are targeted at small-signal monitoring applications and include a 16-bit sigma-delta ADC, dual low-power operational amplifiers, dual 12-bit DACs, voltage comparator, four USCIs (two USCI_A modules and two USCI_B modules), four 16-bit timers, a hardware multiplier, a DMA module, an RTC module, an LCD driver with integrated contrast control for up to 160 segments, an auxiliary supply system, up to 128KB of flash, 10KB of SRAM, and 73 I/O pins in 100-pin devices and 113-pin devices.

Typical applications for these microcontrollers include small signal-monitoring applications such as handheld test and measurement equipment, field transmitters, and blood glucose meters. These microcontrollers can reduce overall system cost through high analog integration and enable long battery life by low-power operation.

The MSP430FG662x and MSP430FG642x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits include the MSP-TS430PZ100AUSB 100-pin target development board. TI also provides free MSP430Ware™ software, which is available as a component of Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer. The MSP430 MCUs are also supported by extensive online collateral, training, and online support through the TI E2E™ support forums.

For complete module descriptions, see the MSP430F5xx and MSP430F6xx Family User's Guide.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE(2)
MSP430FG6626IPZ	PZ (100)	14 mm × 14 mm
MSP430FG6626IZCA	nFBGA (113)	7 mm × 7 mm
MSP430FG6626IZQW(3)	MicroStar Junior™ BGA (113)	7 mm × 7 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 12.

(3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the Product life cycle page for details on this status.

4 Functional Block Diagrams

Figure 4-1 shows the functional block diagram for the MSP430FG6626 and MSP430FG6625 devices.

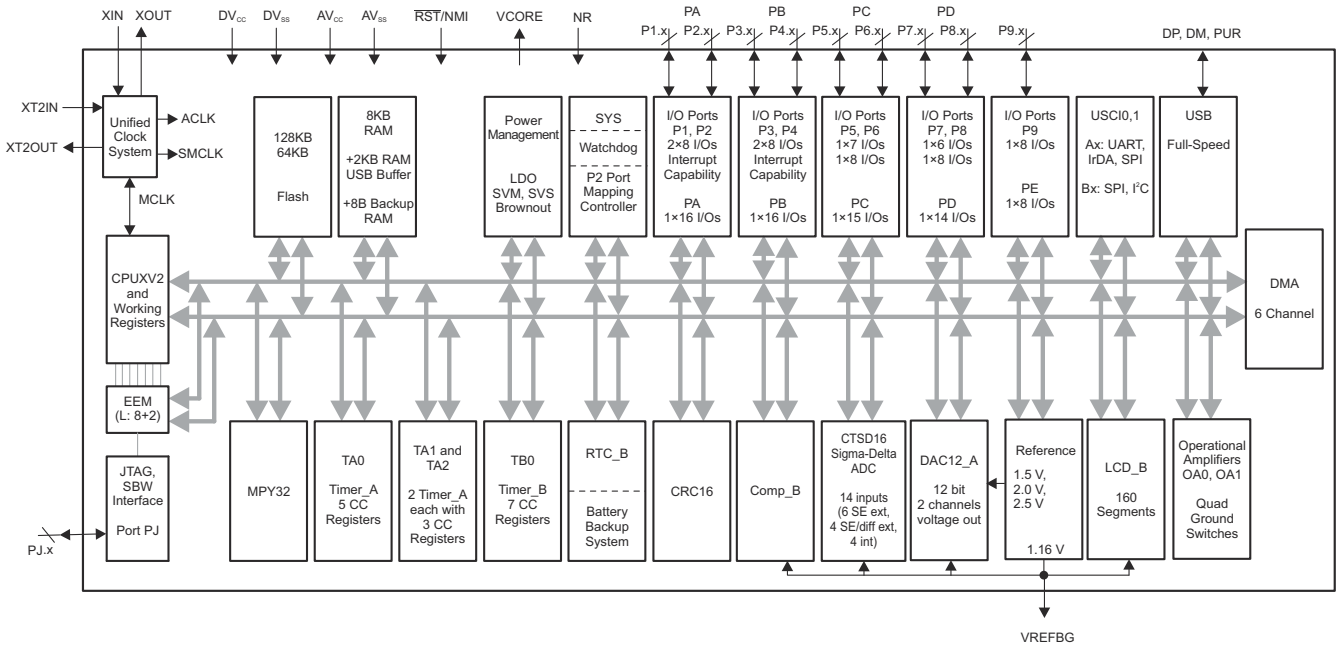

Figure 4-1. Functional Block Diagram – MSP430FG6626, MSP430FG6625

Figure 4-2 shows the functional block diagram for the MSP430FG6426 and MSP430FG6425 devices.

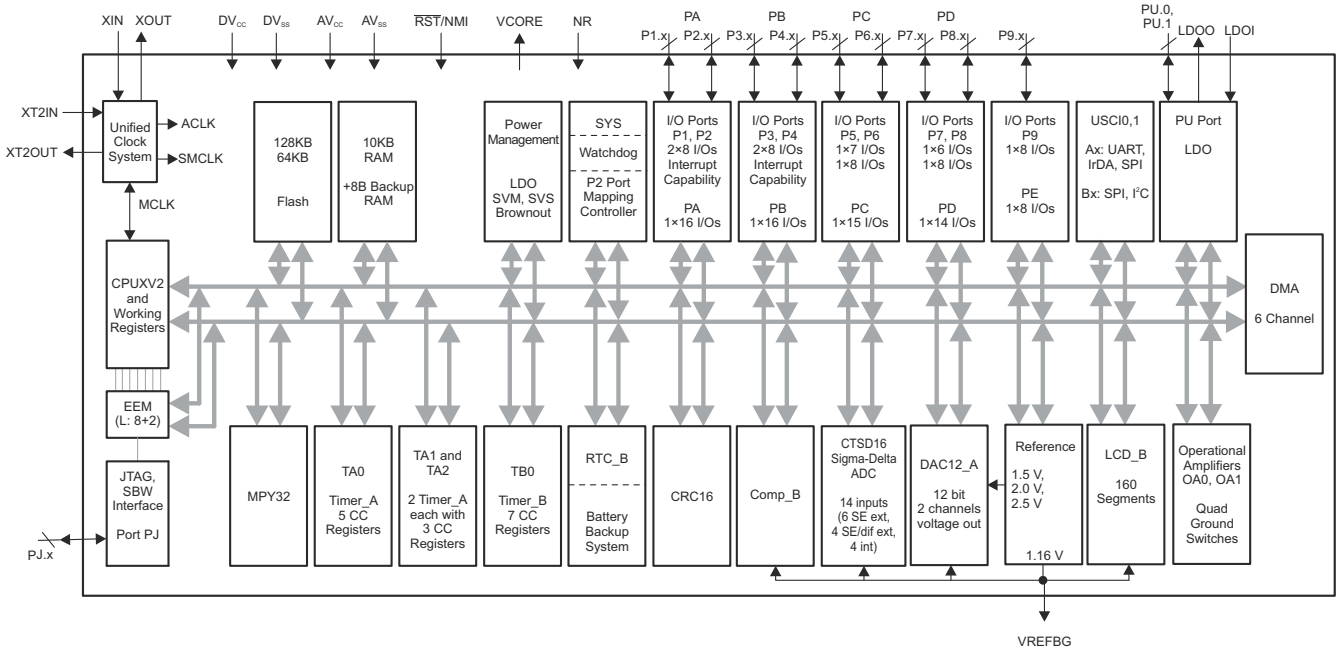

Figure 4-2. Functional Block Diagram – MSP430FG6426, MSP430FG6425

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision A to revision B

Changes from September 27, 2018 to September 11, 2020	Page
• Updated the numbering for sections, tables, figures, and cross-references throughout the document	1
• Updated Section 1, *Features*	1
• Added nFBGA package (ZCA) information throughout document	2
• Added note about status change for all orderable part numbers in the ZQW package in Device Information	2
• Updated Section 3, *Description*	2
• Corrected the signal name and description (changed DVCC to AVCC) on pin 16 (or H1, G2) in Table 7-2, *Signal Descriptions*	18
• Changed the MAX value of the I_{ERASE} and I_{MERASE}, I_{BANK} parameters in Section 8.8.19.1, *Flash Memory*	75

Changes from initial release to revision A

Changes from May 22, 2015 to September 26, 2018	Page
• Added Section 6.1, *Related Products*	7
• Added typical conditions statements at the beginning of Section 8, *Specifications*	27
• Updated notes (1) and (2) and added note (3) in Section 8.8.4.1, *Wake-up Times From Low-Power Modes and Reset*	37
• Removed duplicate symbol and removed note (5) on $Ri_{(VREFBG)}$, $Ri_{(VeREF+)}$ parameter in Section 8.8.13.4, *12-Bit DAC, Reference Input Specifications*	64
• Added "CBPWRMD = 00 or 01" to Test Conditions of the first row of the t_{EN_CMP} parameter; Added second row for t_{EN_CMP} with Test Conditions of "CBPWRMD = 10" and MAX value of 100 µs in Section 8.8.16.1, *Comparator_B*	70
• Added Section 8.8.18, *LDO-PWR (LDO Power System)*	74
• Throughout document, changed all instances of "bootstrap loader" to "bootloader"	85
• Changed decoupling capacitor recommendation from "one 10 µF and one 100 nF" to "one 1 µF and one 100 nF" for consistency with Section 10.1.1	157
• Changed decoupling capacitor recommendation from "one 10 µF and one 100 nF" to "one 1 µF and one 100 nF" for consistency with Section 10.1.1	158
• Changed decoupling capacitor recommendation from "one 10 µF and one 100 nF" to "one 1 µF and one 100 nF" for consistency with Section 10.1.1	161
• Added Section 10.2.5, *DAC12 Peripheral*	165
• Added Section 10.2.6, *USB Module*	166
• Added Section 10.2.7, *LDO Module*	167
• Replaced former section *Development Tools Support* with Section 11.3, *Tools and Software*	170
• Changed format and added content to Section 11.4, *Documentation Support*	172

6 Device Comparison

Table 6-1 summarizes the available family members.

Table 6-1. Device Comparison

DEVICE(1) (2)	FLASH (KB)	SRAM (KB)(3)	Timer_A(4)	Timer_B(5)	USCI_A: UART, IrDA, SPI	USCI_B: SPI, I²C	CTSD16 (Ch)(6)	DAC12_A (Ch)	OA	Comp_B (channels)	USB	I/Os	PACKAGE
MSP430FG6626	128	8 + 2	5, 3, 3	7	2	2	10 ext, 5 int	2	2	12	1	73	100 PZ, 113 ZCA 113 ZQW
MSP430FG6625	64	8 + 2	5, 3, 3	7	2	2	10 ext, 5 int	2	2	12	1	73	100 PZ, 113 ZCA 113 ZQW
MSP430FG6426	128	10	5, 3, 3	7	2	2	10 ext, 5 int	2	2	12	0	73	100 PZ, 113 ZCA 113 ZQW
MSP430FG6425	64	10	5, 3, 3	7	2	2	10 ext, 5 int	2	2	12	0	73	100 PZ, 113 ZCA 113 ZQW

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

(3) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.

(4) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

(5) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

(6) ADC inputs consist of a mix of single ended and differential. See the pinning for available input pairs and types.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI microcontrollers

TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 ultra-low-power microcontrollers

One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Companion products for MSP430FG6626

Review products that are frequently purchased or used with this product.

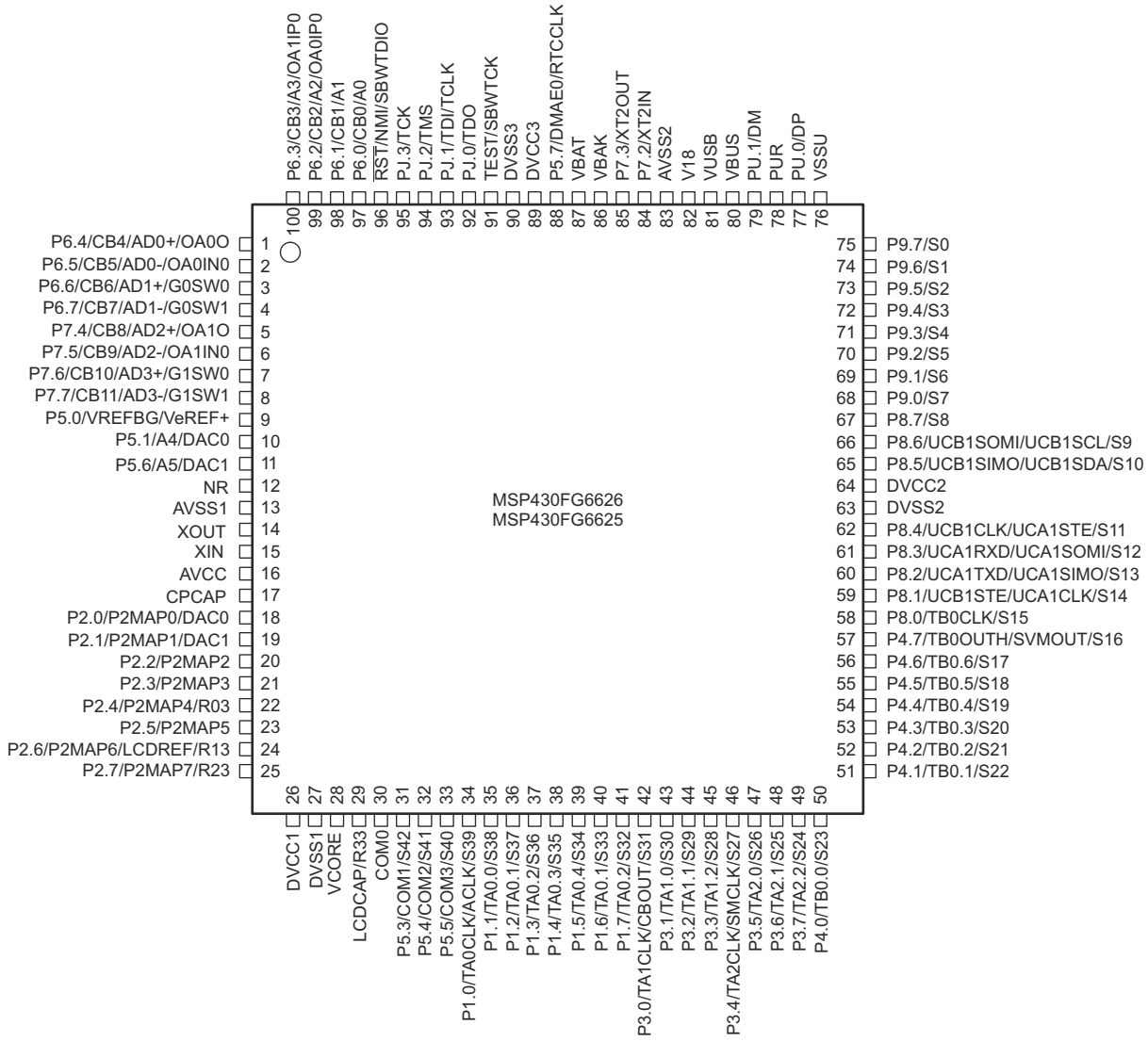
Reference designs for MSP430FG6626

Find reference designs that leverage the best in TI technology to solve your system-level challenges.

7 Terminal Configuration and Functions

7.1 Pin Diagrams

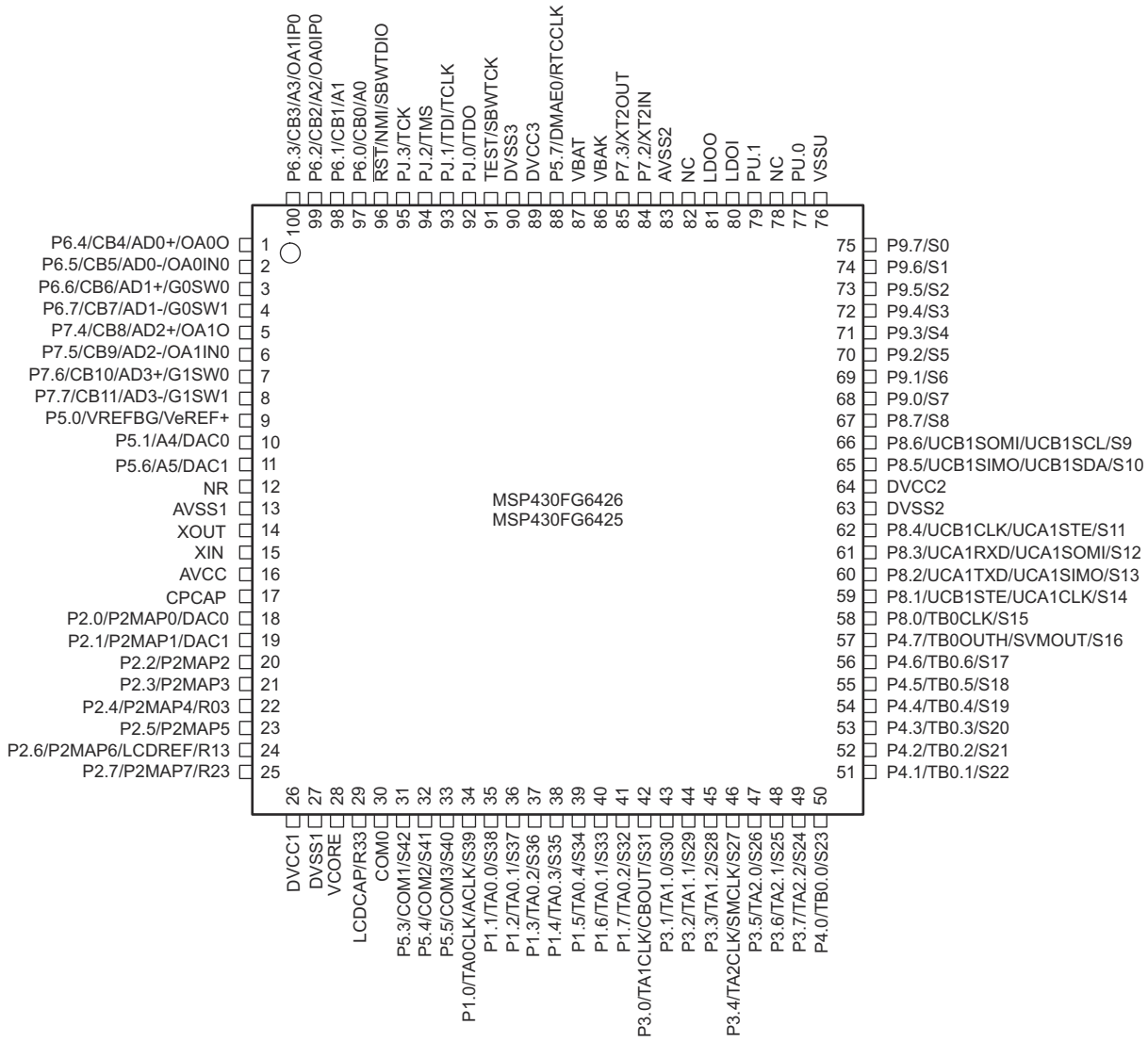
Figure 7-1 shows the pinout for the MSP430FG6626 and MSP430FG6625 devices in the 100-pin PZ package.



CAUTION: LCDCAP/R33 must be connected to DV_{SS} if not used.

Figure 7-1. 100-Pin PZ Package (Top View), MSP430FG6626IPZ, MSP430FG6625IPZ

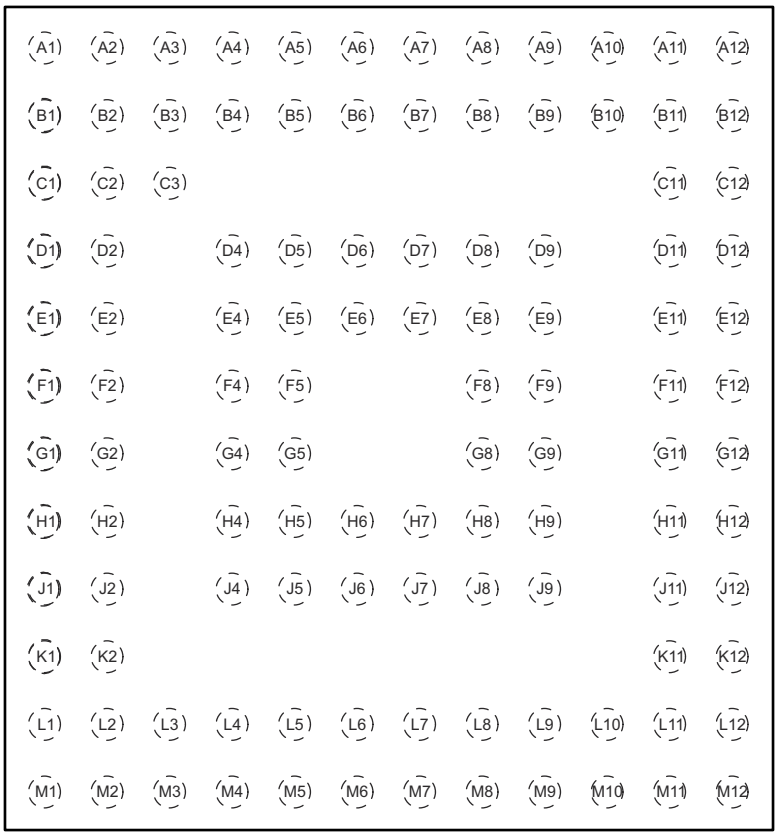
Figure 7-2 shows the pinout for the MSP430FG6426 and MSP430FG6425 devices in the 100-pin PZ package.



A. CAUTION: LCDCAP/R33 must be connected to DV_{SS} if not used.

Figure 7-2. 100-Pin PZ Package (Top View), MSP430FG6426IPZ, MSP430FG6425IPZ

Figure 7-3 shows the pinout for the 113-pin ZCA or ZQW package.



NOTE: For terminal assignments, see Section 7.3.

Figure 7-3. 113-Pin ZCA or ZQW Package (Top View), MSP430FG6626IZCA, MSP430FG6625IZCA, MSP430FG6426IZCA, MSP430FG6425IZCA, MSP430FG6626IZQW, MSP430FG6625IZQW, MSP430FG6426IZQW, MSP430FG6425IZQW

7.2 Pin Attributes

Table 7-1 describes the attributes of the pins.

Table 7-1. Pin Attributes

PIN NO.		SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE(5)	RESET STATE AFTER BOR (6) (7)
PZ	ZCA, ZQW					
1	A1	P6.4	I/O	LVCMOS	DVCC	OFF
		CB4	I	Analog	DVCC	N/A
		AD0+	I	Analog	DVCC	N/A
		OA0O	O	Analog	DVCC	N/A
2	B2	P6.5	I/O	LVCMOS	DVCC	OFF
		CB5	I	Analog	DVCC	N/A
		AD0-	I	Analog	DVCC	N/A
		OA0IN0	I	Analog	DVCC	N/A
3	B1	P6.6	I/O	LVCMOS	DVCC	OFF
		CB6	I	Analog	DVCC	N/A
		AD1+	I	Analog	DVCC	N/A
		G0SW0	I	Analog	DVCC	N/A
4	C3	P6.7	I/O	LVCMOS	DVCC	OFF
		CB7	I	Analog	DVCC	N/A
		AD1-	I	Analog	DVCC	N/A
		G0SW1	I	Analog	DVCC	N/A
5	C2	P7.4	I/O	LVCMOS	DVCC	OFF
		CB8	I	Analog	DVCC	N/A
		AD2+	I	Analog	DVCC	N/A
		OA1O	O	Analog	DVCC	N/A
6	C1	P7.5	I/O	LVCMOS	DVCC	OFF
		CB9	I	Analog	DVCC	N/A
		AD2-	I	Analog	DVCC	N/A
		OA1IN0	I	Analog	DVCC	N/A
7	D4	P7.6	I/O	LVCMOS	DVCC	OFF
		CB10	I	Analog	DVCC	N/A
		AD3+	I	Analog	DVCC	N/A
		G1SW0	I	Analog	DVCC	N/A
8	D2	P7.7	I/O	LVCMOS	DVCC	OFF
		CB11	I	Analog	DVCC	N/A
		AD3-	I	Analog	DVCC	N/A
		G1SW1	I	Analog	DVCC	N/A
9	D1	P5.0	I/O	LVCMOS	DVCC	OFF
		VREFBG	O	Analog	DVCC	N/A
		VeREF+	I	Analog	N/A	N/A
10	E4	P5.1	I/O	LVCMOS	DVCC	OFF
		A4	I	Analog	DVCC	N/A
		DAC0	O	Analog	DVCC	N/A
11	E2	P5.6	I/O	LVCMOS	DVCC	OFF
		A5	I	Analog	DVCC	N/A
		DAC1	O	Analog	DVCC	N/A

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME [1] [2]	SIGNAL TYPE [3]	BUFFER TYPE [4]	POWER SOURCE [5]	RESET STATE AFTER BOR [6] [7]
PZ	ZCA, ZQW					
12	E1	NR	I	Analog	N/A	N/A
13	F2	AVSS1	P	Power	N/A	N/A
14	F1	XOUT	O	Analog	N/A	N/A
15	G1	XIN	I	Analog	N/A	N/A
16	H1, G2	AVCC	P	Power	N/A	N/A
17	G4	CPCAP	I/O	Analog	DVCC	N/A
18	H2	P2.0	I/O	LVCMOS	DVCC	OFF
		P2MAP0	I/O	LVCMOS	DVCC	N/A
		DAC0	O	Analog	DVCC	N/A
19	J1	P2.1	I/O	LVCMOS	DVCC	OFF
		P2MAP1	I/O	LVCMOS	DVCC	N/A
		DAC1	O	Analog	DVCC	N/A
20	H4	P2.2	I/O	LVCMOS	DVCC	OFF
		P2MAP2	I/O	LVCMOS	DVCC	N/A
21	J2	P2.3	I/O	LVCMOS	DVCC	OFF
		P2MAP3	I/O	LVCMOS	DVCC	N/A
22	K1	P2.4	I/O	LVCMOS	DVCC	OFF
		P2MAP4	I/O	LVCMOS	DVCC	N/A
		R03	I/O	Analog	DVCC	N/A
23	K2	P2.5	I/O	LVCMOS	DVCC	OFF
		P2MAP5	I/O	LVCMOS	DVCC	N/A
24	L2	P2.6	I/O	LVCMOS	DVCC	OFF
		P2MAP6	I/O	LVCMOS	DVCC	N/A
		LCDREF	I	Analog	N/A	N/A
		R13	I/O	Analog	DVCC	N/A
25	L3	P2.7	I/O	LVCMOS	DVCC	OFF
		P2MAP7	I/O	LVCMOS	DVCC	N/A
		R23	I/O	Analog	DVCC	N/A
26	L1	DVCC1	P	Power	N/A	N/A
27	M1	DVSS1	P	Power	N/A	N/A
28	M2	VCORE	P	Power	DVCC	N/A
29	M3	LCDCAP	I/O	Analog	DVCC	N/A
		R33	I/O	Analog	DVCC	N/A
30	J4	COM0	O	Analog	DVCC	N/A
31	L4	P5.3	I/O	LVCMOS	DVCC	OFF
		COM1	O	Analog	DVCC	N/A
		S42	O	Analog	DVCC	N/A
32	M4	P5.4	I/O	LVCMOS	DVCC	OFF
		COM2	O	LVCMOS	DVCC	N/A
		S41	O	Analog	DVCC	N/A
33	J5	P5.5	I/O	LVCMOS	DVCC	OFF
		COM3	I/O	LVCMOS	DVCC	N/A
		S40	O	Analog	DVCC	N/A
34	L5	P1.0	I/O	LVCMOS	DVCC	OFF

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE(5)	RESET STATE AFTER BOR (6) (7)
PZ	ZCA, ZQW					
		TA0CLK	I	LVCMOS	DVCC	N/A
		ACLK	O	LVCMOS	DVCC	N/A
		S39	O	Analog	DVCC	N/A
35	M5	P1.1	I/O	LVCMOS	DVCC	OFF
		TA0.0	I/O	LVCMOS	DVCC	N/A
		BSLTX	O	LVCMOS	DVCC	N/A
		S38	O	Analog	DVCC	N/A
36	J6	P1.2	I/O	LVCMOS	DVCC	OFF
		TA0.1	I/O	LVCMOS	DVCC	N/A
		BSLRX	I	LVCMOS	DVCC	N/A
		S37	O	Analog	DVCC	N/A
37	H6	P1.3	I/O	LVCMOS	DVCC	OFF
		TA0.2	I/O	LVCMOS	DVCC	N/A
		S36	O	Analog	DVCC	N/A
38	M6	P1.4	I/O	LVCMOS	DVCC	OFF
		TA0.3	I/O	LVCMOS	DVCC	N/A
		S35	O	Analog	DVCC	N/A
39	L6	P1.5	I/O	LVCMOS	DVCC	OFF
		TA0.4	I/O	LVCMOS	DVCC	N/A
		S34	O	Analog	DVCC	N/A
40	J7	P1.6	I/O	LVCMOS	DVCC	OFF
		TA0.1	I/O	LVCMOS	DVCC	N/A
		S33	O	Analog	DVCC	N/A
41	M7	P1.7	I/O	LVCMOS	DVCC	OFF
		TA0.2	I/O	LVCMOS	DVCC	N/A
		S32	O	Analog	DVCC	N/A
42	L7	P3.0	I/O	LVCMOS	DVCC	OFF
		TA1CLK	I	LVCMOS	DVCC	N/A
		CBOUT	O	LVCMOS	DVCC	N/A
		S31	O	Analog	DVCC	N/A
43	H7	P3.1	I/O	LVCMOS	DVCC	OFF
		TA1.0	I/O	LVCMOS	DVCC	N/A
		S30	O	Analog	DVCC	N/A
44	M8	P3.2	I/O	LVCMOS	DVCC	OFF
		TA1.1	I/O	LVCMOS	DVCC	N/A
		S29	O	Analog	DVCC	N/A
45	L8	P3.3	I/O	LVCMOS	DVCC	OFF
		TA1.2	I/O	LVCMOS	DVCC	N/A
		S28	O	Analog	DVCC	N/A
46	J8	P3.4	I/O	LVCMOS	DVCC	OFF
		TA2CLK	I	LVCMOS	DVCC	N/A
		SMCLK	O	LVCMOS	DVCC	N/A
		S27	O	Analog	DVCC	N/A
47	M9	P3.5	I/O	LVCMOS	DVCC	OFF

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME [1] [2]	SIGNAL TYPE [3]	BUFFER TYPE [4]	POWER SOURCE [5]	RESET STATE AFTER BOR [6] [7]
PZ	ZCA, ZQW					
		TA2.0	I/O	LVCMOS	DVCC	N/A
		S26	O	Analog	DVCC	N/A
48	L9	P3.6	I/O	LVCMOS	DVCC	OFF
		TA2.1	I/O	LVCMOS	DVCC	N/A
		S25	O	Analog	DVCC	N/A
49	M10	P3.7	I/O	LVCMOS	DVCC	OFF
		TA2.2	I/O	LVCMOS	DVCC	N/A
		S24	O	Analog	DVCC	N/A
50	J9	P4.0	I/O	LVCMOS	DVCC	OFF
		TB0.0	I/O	LVCMOS	DVCC	N/A
		S23	O	Analog	DVCC	N/A
51	M11	P4.1	I/O	LVCMOS	DVCC	OFF
		TB0.1	I/O	LVCMOS	DVCC	N/A
		S22	O	Analog	DVCC	N/A
52	L10	P4.2	I/O	LVCMOS	DVCC	OFF
		TB0.2	I/O	LVCMOS	DVCC	N/A
		S21	O	Analog	DVCC	N/A
53	M12	P4.3	I/O	LVCMOS	DVCC	OFF
		TB0.3	I/O	LVCMOS	DVCC	N/A
		S20	O	Analog	DVCC	N/A
54	L12	P4.4	I/O	LVCMOS	DVCC	OFF
		TB0.4	I/O	LVCMOS	DVCC	N/A
		S19	O	Analog	DVCC	N/A
55	L11	P4.5	I/O	LVCMOS	DVCC	OFF
		TB0.5	I/O	LVCMOS	DVCC	N/A
		S18	O	Analog	DVCC	N/A
56	K11	P4.6	I/O	LVCMOS	DVCC	OFF
		TB0.6	I/O	LVCMOS	DVCC	N/A
		S17	O	Analog	DVCC	N/A
57	K12	P4.7	I/O	LVCMOS	DVCC	OFF
		TB0OUTH	I	LVCMOS	DVCC	N/A
		SVMOUT	O	LVCMOS	DVCC	N/A
		S16	O	Analog	DVCC	N/A
58	J11	P8.0	I/O	LVCMOS	DVCC	OFF
		TB0CLK	I	LVCMOS	DVCC	N/A
		S15	O	Analog	DVCC	N/A
59	J12	P8.1	I/O	LVCMOS	DVCC	OFF
		UCB1STE	I/O	LVCMOS	DVCC	N/A
		UCA1CLK	I/O	LVCMOS	DVCC	N/A
		S14	O	Analog	DVCC	N/A
60	H11	P8.2	I/O	LVCMOS	DVCC	OFF
		UCA1TXD	O	LVCMOS	DVCC	N/A
		UCA1SIMO	I/O	LVCMOS	DVCC	N/A
		S13	O	Analog	DVCC	N/A

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE(5)	RESET STATE AFTER BOR (6) (7)
PZ	ZCA, ZQW					
61	H12	P8.3	I/O	LVCMOS	DVCC	OFF
		UCA1RXD	I	LVCMOS	DVCC	N/A
		UCA1SOMI	I/O	LVCMOS	DVCC	N/A
		S12	O	Analog	DVCC	N/A
62	G11	P8.4	I/O	LVCMOS	DVCC	OFF
		UCB1CLK	I/O	LVCMOS	DVCC	N/A
		UCA1STE	I/O	LVCMOS	DVCC	N/A
		S11	O	Analog	DVCC	N/A
63	G12	DVSS2	P	Power	N/A	N/A
64	F12	DVCC2	P	Power	N/A	N/A
65	F11	P8.5	I/O	LVCMOS	DVCC	OFF
		UCB1SIMO	I/O	LVCMOS	DVCC	N/A
		UCB1SDA	I/O	LVCMOS	DVCC	N/A
		S10	O	Analog	DVCC	N/A
66	G9	P8.6	I/O	LVCMOS	DVCC	OFF
		UCB1SOMI	I/O	LVCMOS	DVCC	N/A
		UCB1SCL	I/O	LVCMOS	DVCC	N/A
		S9	O	Analog	DVCC	N/A
67	E12	P8.7	I/O	LVCMOS	DVCC	OFF
		S8	O	Analog	DVCC	N/A
68	E11	P9.0	I/O	LVCMOS	DVCC	OFF
		S7	O	Analog	DVCC	N/A
69	F9	P9.1	I/O	LVCMOS	DVCC	OFF
		S6	O	Analog	DVCC	N/A
70	D12	P9.2	I/O	LVCMOS	DVCC	OFF
		S5	O	Analog	DVCC	N/A
71	D11	P9.3	I/O	LVCMOS	DVCC	OFF
		S4	O	Analog	DVCC	N/A
72	E9	P9.4	I/O	LVCMOS	DVCC	OFF
		S3	O	Analog	DVCC	N/A
73	C12	P9.5	I/O	LVCMOS	DVCC	OFF
		S2	O	Analog	DVCC	N/A
74	C11	P9.6	I/O	LVCMOS	DVCC	OFF
		S1	O	Analog	DVCC	N/A
75	D9	P9.7	I/O	LVCMOS	DVCC	OFF
		S0	O	Analog	DVCC	N/A
76	B11, B12	VSSU	P	Power	N/A	N/A
77	A12	PU.0	I/O	HVCMOS	VBUS	HiZ
		DP	I/O	HVCMOS	VBUS	N/A
78	B10	PUR (FG662x only)	I/O	HVCMOS/open-drain	VBUS	HiZ
		NC (FG642x only)	I/O	N/A	N/A	N/A
79	A11	PU.1	I/O	HVCMOS	VBUS	HiZ
		DM	I/O	HVCMOS	VBUS	N/A

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE(5)	RESET STATE AFTER BOR (6) (7)
PZ	ZCA, ZQW					
80	A10	VBUS	I	Power	N/A	N/A
		LDOI	I	Analog	External	N/A
81	A9	VUSB	O	Power	N/A	N/A
		LDOO	O	Analog	VBUS	N/A
82	B9	V18 (FG662x only)	O	Power	N/A	N/A
		NC (FG642x only)	–	N/A	N/A	N/A
83	A8	AVSS2	P	Power	N/A	N/A
84	B8	P7.2	I/O	LVCMOS	DVCC	OFF
		XT2IN	I	Analog	DVCC	N/A
85	B7	P7.3	I/O	LVCMOS	DVCC	OFF
		XT2OUT	O	Analog	DVCC	N/A
86	A7	VBAK	I/O	Analog	N/A	N/A
87	D8	VBAT	P	Power	N/A	N/A
88	D7	P5.7	I/O	LVCMOS	DVCC	OFF
		DMAE0	I	LVCMOS	DVCC	N/A
		RTCCLK	O	LVCMOS	DVCC	N/A
89	A6	DVCC3	P	Power	N/A	N/A
90	A5	DVSS3	P	Power	N/A	N/A
91	B6	TEST	I	LVCMOS	DVCC	No Emu: PD Emu: PD
		SBWTCK	I	LVCMOS	DVCC	N/A
92	B5	PJ.0	I/O	LVCMOS	DVCC	OFF
		TDO	O	LVCMOS	DVCC	No Emu: OFF Emu: DRIVE0
93	A4	PJ.1	I/O	LVCMOS	DVCC	OFF
		TDI	I	LVCMOS	DVCC	No Emu: OFF Emu: PU
		TCLK	I	LVCMOS	DVCC	No Emu: OFF Emu: OFF
94	E7	PJ.2	I/O	LVCMOS	DVCC	OFF
		TMS	I	LVCMOS	DVCC	No Emu: OFF Emu: PU
95	D6	PJ.3	I/O	LVCMOS	DVCC	OFF
		TCK	I	LVCMOS	DVCC	No Emu: OFF Emu: PU
96	A3	$\overline{\text{RST}}$	I/O	LVCMOS	DVCC	PU
		NMI	I	LVCMOS	DVCC	N/A
		SBWTDIO	I/O	LVCMOS	DVCC	PU
97	B4	P6.0	I/O	LVCMOS	DVCC	OFF
		CB0	I	Analog	DVCC	N/A
		A0	I	Analog	DVCC	N/A
98	B3	P6.1	I/O	LVCMOS	DVCC	OFF
		CB1	I	Analog	DVCC	N/A
		A1	I	Analog	DVCC	N/A
99	A2	P6.2	I/O	LVCMOS	DVCC	OFF
		CB2	I	Analog	DVCC	N/A

Table 7-1. Pin Attributes (continued)

PIN NO.		SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE(5)	RESET STATE AFTER BOR (6) (7)
PZ	ZCA, ZQW					
		A2	I	Analog	DVCC	N/A
		OA0IP0	I	Analog	DVCC	N/A
100	D5	P6.3	I/O	LVCMOS	DVCC	OFF
		CB3	I	Analog	DVCC	N/A
		A3	I	Analog	DVCC	N/A
		OA1IP0	I	Analog	DVCC	N/A
N/A	E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9	Reserved	-	–	–	–

(1) For each multiplexed pin, the signal that is listed first in this table is the reset default.
(2) To determine the pin mux encodings for each pin, refer to Section 9.13.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power
(4) Buffer Types: LVCMOS, HVCMOS, Analog, or Power (see Table 7-3 for details).
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
HiZ = High-impedance (neither input nor output)
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
DRIVE0 = Drive output low
DRIVE1 = Drive output high
N/A = Not applicable
(7) For Debug pins: Emu = with emulator attached at reset, No Emu = without emulator attached at reset

7.3 Signal Descriptions

Table 7-2 describes the signals for all device variants and package options.

Table 7-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE(1)	DESCRIPTION
		PZ	ZCA, ZQW		
ADC	A0	97	B4	I	ADC analog single ended input A0
	A1	98	B3	I	ADC analog single ended input A1
	A2	99	A2	I	ADC analog single ended input A2
	A3	100	D5	I	ADC analog single ended input A3
	A4	10	E4	I	ADC analog single ended input A4
	A5	11	E2	I	ADC analog single ended input A5
	AD0+	1	A1	I	ADC positive analog differential input AD0+
	AD0-	2	B2	I	ADC negative analog differential input AD0-
	AD1+	3	B1	I	ADC positive analog differential input AD1+
	AD1-	4	C3	I	ADC negative analog differential input AD1-
	AD2+	5	C2	I	ADC positive analog differential input AD2+
	AD2-	6	C1	I	ADC negative analog differential input AD2-
	AD3+	7	D4	I	ADC positive analog differential input AD3+
	AD3-	8	D2	I	ADC negative analog differential input AD3-
	VeREF+	9	D1	I	Input for an external reference voltage to the ADC and DAC
BSL	BSLRX	36	J6	I	BSL receive input
	BSLTX	35	M5	O	BSL transmit output
Backup	VBAK	86	A7	I/O	Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see C_{BAK} in Section 8.3.
	VBAT	87	D8	P	Backup or secondary supply voltage. If backup voltage is not supplied, connect to DVCC externally.
Charge Pump	CPCAP	17	G4	I/O	Capacitor for op amp and CTSD16 rail-to-rail charge pump
Clock	ACLK	34	L5	O	ACLK output (divided by 1, 2, 4, 8, 16, or 32)
	RTCCLK	88	D7	O	RTCCLK output
	SMCLK	46	J8	O	SMCLK output
	XIN	15	G1	I	Input terminal for crystal oscillator XT1
	XOUT	14	F1	O	Output terminal of crystal oscillator XT1
	XT2IN	84	B8	I	Input terminal for crystal oscillator XT2
	XT2OUT	85	B7	O	Output terminal of crystal oscillator XT2
Comparator	CB0	97	B4	I	Comparator_B input CB0
	CB1	98	B3	I	Comparator_B input CB1
	CB2	99	A2	I	Comparator_B input CB2
	CB3	100	D5	I	Comparator_B input CB3
	CB4	1	A1	I	Comparator_B input CB4
	CB5	2	B2	I	Comparator_B input CB5
	CB6	3	B1	I	Comparator_B input CB6
	CB7	4	C3	I	Comparator_B input CB7
	CB8	5	C2	I	Comparator_B input CB8
	CB9	6	C1	I	Comparator_B input CB9
	CB10	7	D4	I	Comparator_B input CB10
	CB11	8	D2	I	Comparator_B input CB11
	CBOUT	42	L7	O	Comparator_B output

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
DAC	DAC0	10 18	E4 H2	O	DAC output channel 0
	DAC1	11 19	E2 J1	O	DAC output channel 1
DMA	DMAE0	88	D7	I	DMA external trigger input
Debug	SBWTCK	91	B6	I	Spy-Bi-Wire input clock
	TCK	95	D6	I	Test clock
	TCLK	93	A4	I	Test clock input
	TDI	93	A4	I	Test data input
	TDO	92	B5	O	Test data output
	TEST	91	B6	I	Test mode pin; selects digital I/O on JTAG pins
	TMS	94	E7	I	Test mode select
	SBWTDIO	96	A3	I/O	Spy-Bi-Wire data input/output
GPIO	P1.0	34	L5	I/O	General-purpose digital I/O with port interrupt
	P1.1	35	M5	I/O	General-purpose digital I/O with port interrupt
	P1.2	36	J6	I/O	General-purpose digital I/O with port interrupt
	P1.3	37	H6	I/O	General-purpose digital I/O with port interrupt
	P1.4	38	M6	I/O	General-purpose digital I/O with port interrupt
	P1.5	39	L6	I/O	General-purpose digital I/O with port interrupt
	P1.6	40	J7	I/O	General-purpose digital I/O with port interrupt
	P1.7	41	M7	I/O	General-purpose digital I/O with port interrupt
	P2.0	18	H2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.1	19	J1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.2	20	H4	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.3	21	J2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.4	22	K1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.5	23	K2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.6	24	L2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P2.7	25	L3	I/O	General-purpose digital I/O with port interrupt and mappable secondary function
	P3.0	42	L7	I/O	General-purpose digital I/O with port interrupt
	P3.1	43	H7	I/O	General-purpose digital I/O with port interrupt
	P3.2	44	M8	I/O	General-purpose digital I/O with port interrupt
	P3.3	45	L8	I/O	General-purpose digital I/O with port interrupt
	P3.4	46	J8	I/O	General-purpose digital I/O with port interrupt
	P3.5	47	M9	I/O	General-purpose digital I/O with port interrupt
	P3.6	48	L9	I/O	General-purpose digital I/O with port interrupt
	P3.7	49	M10	I/O	General-purpose digital I/O with port interrupt
GPIO	P4.0	50	J9	I/O	General-purpose digital I/O with port interrupt

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
	P4.1	51	M11	I/O	General-purpose digital I/O with port interrupt
	P4.2	52	L10	I/O	General-purpose digital I/O with port interrupt
	P4.3	53	M12	I/O	General-purpose digital I/O with port interrupt
	P4.4	54	L12	I/O	General-purpose digital I/O with port interrupt
	P4.5	55	L11	I/O	General-purpose digital I/O with port interrupt
	P4.6	56	K11	I/O	General-purpose digital I/O with port interrupt
	P4.7	57	K12	I/O	General-purpose digital I/O with port interrupt
	P5.0	9	D1	I/O	General-purpose digital I/O
	P5.1	10	E4	I/O	General-purpose digital I/O
	P5.3	31	L4	I/O	General-purpose digital I/O
	P5.4	32	M4	I/O	General-purpose digital I/O
	P5.5	33	J5	I/O	General-purpose digital I/O
	P5.6	11	E2	I/O	General-purpose digital I/O
	P5.7	88	D7	I/O	General-purpose digital I/O
	P6.0	97	B4	I/O	General-purpose digital I/O
	P6.1	98	B3	I/O	General-purpose digital I/O
	P6.2	99	A2	I/O	General-purpose digital I/O
	P6.3	100	D5	I/O	General-purpose digital I/O
	P6.4	1	A1	I/O	General-purpose digital I/O
	P6.5	2	B2	I/O	General-purpose digital I/O
	P6.6	3	B1	I/O	General-purpose digital I/O
	P6.7	4	C3	I/O	General-purpose digital I/O
	P7.2	84	B8	I/O	General-purpose digital I/O
	P7.3	85	B7	I/O	General-purpose digital I/O
	P7.4	5	C2	I/O	General-purpose digital I/O
	P7.5	6	C1	I/O	General-purpose digital I/O
	P7.6	7	D4	I/O	General-purpose digital I/O
	P7.7	8	D2	I/O	General-purpose digital I/O
	P8.0	58	J11	I/O	General-purpose digital I/O
	P8.1	59	J12	I/O	General-purpose digital I/O
	P8.2	60	H11	I/O	General-purpose digital I/O
	P8.3	61	H12	I/O	General-purpose digital I/O
	P8.4	62	G11	I/O	General-purpose digital I/O
	P8.5	65	F11	I/O	General-purpose digital I/O
	P8.6	66	G9	I/O	General-purpose digital I/O
	P8.7	67	E12	I/O	General-purpose digital I/O
GPIO	P9.0	68	E11	I/O	General-purpose digital I/O
	P9.1	69	F9	I/O	General-purpose digital I/O
	P9.2	70	D12	I/O	General-purpose digital I/O
	P9.3	71	D11	I/O	General-purpose digital I/O
	P9.4	72	E9	I/O	General-purpose digital I/O
	P9.5	73	C12	I/O	General-purpose digital I/O
	P9.6	74	C11	I/O	General-purpose digital I/O
	P9.7	75	D9	I/O	General-purpose digital I/O

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
	PJ.0	92	B5	I/O	General-purpose digital I/O
	PJ.1	93	A4	I/O	General-purpose digital I/O
	PJ.2	94	E7	I/O	General-purpose digital I/O
	PJ.3	95	D6	I/O	General-purpose digital I/O
	PU.0	77	A12	I/O	General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register
	PU.1	79	A11	I/O	General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register
Ground Switch	G0SW0	3	B1	I	Analog switch to AVSS. Internally connected to ADC positive analog differential input AD1+.
	G0SW1	4	C3	I	Analog switch to AVSS. Internally connected to ADC negative analog differential input AD1-.
	G1SW0	7	D4	I	Analog switch to AVSS. Internally connected to ADC positive analog differential input AD3+.
	G1SW1	8	D2	I	Analog switch to AVSS. Internally connected to ADC negative analog differential input AD3-.
I^2C	UCB1SCL	66	G9	I/O	USCI_B1 I^2C clock
	UCB1SDA	65	F11	I/O	USCI_B1 I^2C data
LCD	COM0	30	J4	O	LCD common output COM0 for LCD backplane
	COM1	31	L4	O	LCD common output COM1 for LCD backplane
	COM2	32	M4	O	LCD common output COM2 for LCD backplane
	COM3	33	J5	I/O	LCD common output COM3 for LCD backplane
	LCDCAP	29	M3	I/O	LCD capacitor connection **CAUTION:** LCDCAP/R33 must be connected to DV_{SS} if not used.
	LCDREF	24	L2	I	External reference voltage input for regulated LCD voltage
	R03	22	K1	I/O	Input/output port of lowest analog LCD voltage (V5)
	R13	24	L2	I/O	Input/output port of third most positive analog LCD voltage (V3 or V4)
	R23	25	L3	I/O	Input/output port of second most positive analog LCD voltage (V2)
	R33	29	M3	I/O	Input/output port of most positive analog LCD voltage (V1) **CAUTION:** LCDCAP/R33 must be connected to DV_{SS} if not used.
	S0	75	D9	O	LCD segment output S0
	S1	74	C11	O	LCD segment output S1
	S2	73	C12	O	LCD segment output S2
	S3	72	E9	O	LCD segment output S3
	S4	71	D11	O	LCD segment output S4
	S5	70	D12	O	LCD segment output S5
	S6	69	F9	O	LCD segment output S6
LCD	S7	68	E11	O	LCD segment output S7
	S8	67	E12	O	LCD segment output S8
	S9	66	G9	O	LCD segment output S9
	S10	65	F11	O	LCD segment output S10
	S11	62	G11	O	LCD segment output S11
	S12	61	H12	O	LCD segment output S12
	S13	60	H11	O	LCD segment output S13
	S14	59	J12	O	LCD segment output S14
	S15	58	J11	O	LCD segment output S15

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
	S16	57	K12	O	LCD segment output S16
	S17	56	K11	O	LCD segment output S17
	S18	55	L11	O	LCD segment output S18
	S19	54	L12	O	LCD segment output S19
	S20	53	M12	O	LCD segment output S20
	S21	52	L10	O	LCD segment output S21
	S22	51	M11	O	LCD segment output S22
	S23	50	J9	O	LCD segment output S23
	S24	49	M10	O	LCD segment output S24
	S25	48	L9	O	LCD segment output S25
	S26	47	M9	O	LCD segment output S26
	S27	46	J8	O	LCD segment output S27
	S28	45	L8	O	LCD segment output S28
	S29	44	M8	O	LCD segment output S29
	S30	43	H7	O	LCD segment output S30
	S31	42	L7	O	LCD segment output S31
	S32	41	M7	O	LCD segment output S32
	S33	40	J7	O	LCD segment output S33
	S34	39	L6	O	LCD segment output S34
	S35	38	M6	O	LCD segment output S35
	S36	37	H6	O	LCD segment output S36
	S37	36	J6	O	LCD segment output S37
	S38	35	M5	O	LCD segment output S38
	S39	34	L5	O	LCD segment output S39
	S40	33	J5	O	LCD segment output S40
	S41	32	M4	O	LCD segment output S41
	S42	31	L4	O	LCD segment output S42
Mappable	P2MAP0	18	H2	I/O	Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output Mapping Options: See Table 9-8
	P2MAP1	19	J1	I/O	Default mapping: USCI_B0 SPI slave in/master out; USCI_B0 I^2C data Mapping Options: See Table 9-8
	P2MAP2	20	H4	I/O	Default mapping: USCI_B0 SPI slave out/master in; USCI_B0 I^2C clock Mapping Options: See Table 9-8
	P2MAP3	21	J2	I/O	Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable Mapping Options: See Table 9-8
	P2MAP4	22	K1	I/O	Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in/master out Mapping Options: See Table 9-8
	P2MAP5	23	K2	I/O	Default mapping: USCI_A0 UART receive data; USCI_A0 slave out/master in Mapping Options: See Table 9-8
	P2MAP6	24	L2	I/O	Default mapping: no secondary function Mapping Options: See Table 9-8
	P2MAP7	25	L3	I/O	Default mapping: no secondary function Mapping Options: See Table 9-8

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
Noise Reduction	NR	12	E1	I	Noise reduction. Connect pin to analog ground.
Op Amp	OA1IN0	6	C1	I	OA1 negative input internally connected to ADC negative analog differential input AD2-
	OA0IN0	2	B2	I	OA0 negative input internally connected to ADC negative analog differential input AD0-
	OA0IP0	99	A2	I	OA0 positive input internally connected to ADC analog input A2
	OA0O	1	A1	O	OA0 output internally connected to ADC positive analog differential input AD0+
	OA1IP0	100	D5	I	OA1 positive input internally connected to ADC analog input A3
	OA1O	5	C2	O	OA1 output internally connected to ADC positive analog differential input AD2+
Power	AVSS1	13	F2	P	Analog ground supply
	AVSS2	83	A8	P	Analog ground supply
	AVCC	16	H1, G2	P	Analog power supply
	DVCC1	26	L1	P	Digital power supply
	DVCC2	64	F12	P	Digital power supply
	DVCC3	89	A6	P	Digital power supply
	DVSS1	27	M1	P	Digital ground supply
	DVSS2	63	G12	P	Digital ground supply
	DVSS3	90	A5	P	Digital ground supply
	LDOI	80	A10	I	LDO input (not available on FG662x devices)
	LDOO	81	A9	O	LDO output (not available on FG662x devices)
	VCORE[2]	28	M2	O	Regulated core power supply (internal use only, no external current loading)
REF	VREFBG	9	D1	O	Output of reference voltage to the ADC and DAC
Reserved	NC	78 82	B10 B9	I/O	Not connected (not available on FG662x devices)
	Reserved	–	E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9	–	Reserved. Internally connected to DVSS. TI recommends external connection to ground (DVSS).
SPI	UCA1CLK	59	J12	I/O	USCI_A1 clock input/output
	UCA1SIMO	60	H11	I/O	USCI_A1 SPI slave in/master out
	UCA1SOMI	61	H12	I/O	USCI_A1 SPI slave out/master in
	UCA1STE	62	G11	I/O	USCI_A1 SPI slave transmit enable
	UCB1CLK	62	G11	I/O	USCI_B1 clock input/output
	UCB1SIMO	65	F11	I/O	USCI_B1 SPI slave in/master out
	UCB1SOMI	66	G9	I/O	USCI_B1 SPI slave out/master in
	UCB1STE	59	J12	I/O	USCI_B1 SPI slave transmit enable
System	NMI	96	A3	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	96	A3	I/O	Reset input (active low)[3]
	SVMOUT	57	K12	O	SVM output
Timer_A	TA0.0	35	M5	I/O	Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output
	TA0.1	36	J6	I/O	Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.		PIN TYPE[1]	DESCRIPTION
		PZ	ZCA, ZQW		
		40	J7	I/O	Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output
	TA0.2	37	H6	I/O	Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output
		41	M7	I/O	Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output
	TA0.3	38	M6	I/O	Timer TA0 CCR3 capture: CCI3A input compare: Out3 output
	TA0.4	39	L6	I/O	Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output
	TA0CLK	34	L5	I	Timer TA0 clock signal TACLK input
	TA1.0	43	H7	I/O	Timer TA1 capture CCR0: CCI0A input, compare: Out0 output
	TA1.1	44	M8	I/O	Timer TA1 capture CCR1: CCI1A input, compare: Out1 output
	TA1.2	45	L8	I/O	Timer TA1 capture CCR2: CCI2A input, compare: Out2 output
	TA1CLK	42	L7	I	Timer TA1 clock input
	TA2.0	47	M9	I/O	Timer TA2 capture CCR0: CCI0A input, compare: Out0 output
	TA2.1	48	L9	I/O	Timer TA2 capture CCR1: CCI1A input, compare: Out1 output
	TA2.2	49	M10	I/O	Timer TA2 capture CCR2: CCI2A input, compare: Out2 output
	TA2CLK	46	J8	I	Timer TA2 clock input
Timer_B	TB0.0	50	J9	I/O	Timer TB0 capture CCR0: CCI0A input, compare: Out0 output
	TB0.1	51	M11	I/O	Timer TB0 capture CCR1: CCI1A input, compare: Out1 output
	TB0.2	52	L10	I/O	Timer TB0 capture CCR2: CCI2A input, compare: Out2 output
	TB0.3	53	M12	I/O	Timer TB0 capture CCR3: CCI3A input, compare: Out3 output
	TB0.4	54	L12	I/O	Timer TB0 capture CCR4: CCI4A input, compare: Out4 output
	TB0.5	55	L11	I/O	Timer TB0 capture CCR5: CCI5A input, compare: Out5 output
	TB0.6	56	K11	I/O	Timer TB0 capture CCR6: CCI6A input, compare: Out6 output
	TB0CLK	58	J11	I	Timer TB0 clock input
	TB0OUTH	57	K12	I	Timer TB0: switch all PWM outputs to high impedance
UART	UCA1CLK	59	J12	I/O	USCI_A1 clock input/output
	UCA1RXD	61	H12	I	USCI_A1 UART receive data
	UCA1TXD	60	H11	O	USCI_A1 UART transmit data
USB (FG662x only)	DM	79	A11	I/O	USB data terminal DM (not available on FG6426 and FG6425 devices)
	DP	77	A12	I/O	USB data terminal DP (not available on FG6426 and FG6425 devices)
	PUR	78	B10	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See Section 9.6 for more information. Not available on FG6426 and FG6425 devices.
	V18	82	B9	O	USB regulated power (internal use only, no external current loading) (not available on FG6426 and FG6425 devices)
	VBUS	80	A10	I	USB LDO input (connect to USB power source) (not available on FG6426 and FG6425 devices)
	VSSU	76	B11 B12	P	USB PHY ground supply
	VUSB	81	A9	O	USB LDO output (not available on FG6426 and FG6425 devices)

(1) I = input, O = output, I/O = input or output, P = power
(2) VCORE is for internal use only. No external current loading is possible. VCORE must be connected to the recommended capacitor value, C_{VCORE}.
(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

7.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 9.13.

7.5 Buffer Type

Table 7-3 describes the buffer types that are referenced in Table 7-1.

Table 7-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog(2)	3.0 V	N	N/A	N/A	N/A	See analog modules in Section 8, *Specifications* for details
HVCMOS	5.0 V	Y	N/A	N/A	See Section 8.8.5.7, *Typical Characteristics – Outputs*	
LVCMOS	3.0 V	Y(1)	Programmable	See Section 8.8.5, *General-Purpose I/Os*	See Section 8.8.5.7, *Typical Characteristics – Outputs*	
Power (DVCC)(3)	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC
Power (AVCC)(3)	3.0 V	N	N/A	N/A	N/A	
Power (DVSS and AVSS)(3)	0 V	N	N/A	N/A	N/A	

(1) Only for input pins
(2) This is a switch, not a buffer.
(3) This is supply input, not a buffer.

7.6 Connection of Unused Pins

Table 7-4 lists the correct termination of all unused pins.

Table 7-4. Connection of Unused Pins

(1)PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
AVSS	DV_{SS}	
CPCAP	Open	For devices where the charge pump is not used (no rail-to-rail OA and no rail-to-rail CTSD16).
LCDCAP	DV_{SS}	
LDOI	DV_{SS}	For devices with LDO-PWR module when not being used in the application.
LDOO	Open	For devices with LDO-PWR module when not being used in the application.
NC	Open	
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these must be switched to port function, output direction (PJDIR.n = 1). When used as JTAG pins, these pins must remain open.
PU.0/DP PU.1/DM	Open	For USB devices only when USB module is not being used in the application
PUR(3)	DV_{SS}	For USB devices only when USB module is not being used in the application
Px.y	Open	Switched to port function, output direction (PxDIR.n = 1). Px.y represents port x and bit y of port x (for example, P1.0, P1.1, P2.2, PJ.0, PJ.1)
$\overline{RST}$/NMI	DV_{CC} or V_{CC}	47-kΩ pullup or internal pullup selected with 10-nF (2.2 nF) pulldown(2)
Reserved	DV_{SS}	
TEST	Open	This pin always has an internal pulldown enabled.
V18	Open	For USB devices only when USB module is not being used in the application
VBAK	Open	For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1.
VBAT	DV_{CC}	For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1.
VBUS, VSSU	DV_{SS}	For USB devices only when USB module is not being used in the application
VUSB	Open	For USB devices only when USB module is not being used in the application
XIN	DV_{SS}	For dedicated XIN pins only. XIN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.
XOUT	Open	For dedicated XOUT pins only. XOUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.
XT2IN	DV_{SS}	For dedicated XT2IN pins only. XT2IN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.
XT2OUT	Open	For dedicated XT2OUT pins only. XT2OUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.y unused pin connection guidelines.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools such as FET interfaces or GANG programmers.

(3) The default USB BSL evaluates the state of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends a 1-MΩ resistor to ground.

8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

(1)	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE, VBUS, V18, LDOI) (2)	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (3)	–55	150	°C
Maximum junction temperature, T_J		95	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.

(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

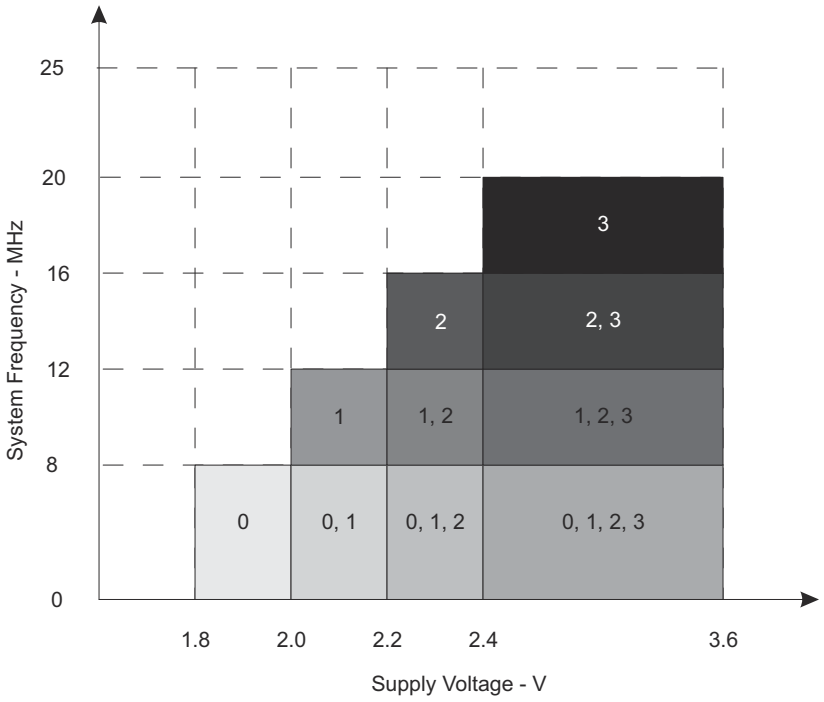
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AVCC = DVCC1 = DVCC2 = DVCC3 = DV_{CC} = V_{CC}) (1) (2) (3)	PMMCOREV = 0	1.8		3.6	V
		PMMCOREV = 0, 1	2.0		3.6	
		PMMCOREV = 0, 1, 2	2.2		3.6	
		PMMCOREV = 0, 1, 2, 3	2.4		3.6	
$V_{CC,USB}$ (2)	Supply voltage during USB operation, USB PLL disabled (USB_EN = 1, UPLLEN = 0)	PMMCOREV = 0	1.8		3.6	V
		PMMCOREV = 0, 1	2.0		3.6	
		PMMCOREV = 0, 1, 2	2.2		3.6	
		PMMCOREV = 0, 1, 2, 3	2.4		3.6	
	Supply voltage during USB operation, USB PLL enabled (4) (USB_EN = 1, UPLLEN = 1)	PMMCOREV = 2	2.2		3.6	
		PMMCOREV = 2, 3	2.4		3.6	
V_{SS}	Supply voltage (AVSS1 = AVSS2 = AVSS3 = DVSS1 = DVSS2 = DVSS3 = V_{SS})			0		V
$V_{BAT,RTC}$	Backup-supply voltage with RTC operational	T_A = 0°C to 85°C	1.55		3.6	V
		T_A = –40°C to 85°C	1.70		3.6	
$V_{BAT,MEM}$	Backup-supply voltage with backup memory retained	T_A = –40°C to 85°C	1.20		3.6	V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
C_{BAK}	Capacitance at pin VBAK		1	4.7	10	nF

8.3 Recommended Operating Conditions (continued)

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
C_{VCORE}	Capacitor at VCORE(5)			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) (6) (7) (see Figure 8-1)	PMMCOREV = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREV = 1, 2 V ≤ V_{CC} ≤ 3.6 V	0		12.0	
		PMMCOREV = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		16.0	
		PMMCOREV = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		20.0	
f_{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5			MHz
USB_wait	Wait state cycles during USB operation			16		cycles

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) Some modules may have reduced recommended ranges of operation.
(3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in Section 8.8.6.2 for the exact values and further details.
(4) USB operation with USB PLL enabled requires PMMCOREV ≥ 2 for proper operation.
(5) A capacitor tolerance of ±20% is required.
(6) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(7) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 8-1. Frequency vs Supply Voltage

8.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREV	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)								UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3 V	0	0.31	0.36	2.0	2.4					mA
			1	0.35		2.3		3.4	4.0			
			2	0.37		2.5		3.8				
			3	0.4		2.7		4.0		6.6		
$I_{AM, RAM}$	RAM	3 V	0	0.2	0.23	1.1	1.2					mA
			1	0.22		1.3		1.9	2.1			
			2	0.24		1.5		2.2				
			3	0.26		1.6		2.4		3.9		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Characterized with program executing typical data processing. FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

8.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREV	TEMPERATURE (T_A)								UNIT
				–40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3) (9)	2.2 V	0	72		77	87	81		87	98	µA
		3 V	3	86		92	105	97		104	117	
I_{LPM2}	Low-power mode 2(4) (9)	2.2 V	0	6.9		7.5	9.9	8.5		12	17	µA
		3 V	3	7.9		8.5	11	9.7		14	20	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(5) (9)	2.2 V	0	2.8		3.2	3.7	4.2		7.6	13.5	µA
			1	3.1		3.6		4.6		8.2		
			2	3.5		4.0		5.1		8.8		
		3 V	0	3.0		3.4	4.0	4.4		7.9	14	
			1	3.3		3.8		4.9		8.5		
			2	3.7		4.2		5.3		9.0		
			3	3.7		4.2	4.8	5.3		9.1	16	
$I_{LPM3,VLO,WDT}$	Low-power mode 3, VLO mode, Watchdog enabled(6) (9)	3 V	0	1.2		1.5	2.1	2.4		5.8	12.5	µA
			1	1.4		1.6		2.6		6.1		
			2	1.6		1.8		2.8		6.5		
			3	1.6		1.8	2.6	2.9		6.5	14	
I_{LPM4}	Low-power mode 4(7) (9)	3 V	0	0.6		0.9	1.8	1.9		5.4	11.5	µA
			1	0.7		1.0		2.0		5.6		
			2	0.8		1.1		2.2		5.9		
			3	0.8		1.1	2.1	2.2		6.0	13	
$I_{LPM3.5,RTC,VCC}$	Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin DV_{CC} (10)	3 V				0.2				0.7	1.7	µA
$I_{LPM3.5,RTC,VBAT}$	Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT(11)	3 V				0.7				0.9	1.2	µA
$I_{LPM3.5,RTC,TOT}$	Total low-power mode 3.5 (LPM3.5) current with active RTC(12)	3 V		0.8		0.9		1.0		1.6	2.9	µA
$I_{LPM4.5}$	Low-power mode 4.5 (LPM4.5)(8)	3 V		0.12		0.2	0.6	0.32		0.8	1.9	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(4) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(6) Current for watchdog timer clocked by VLO included.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz

FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(7) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz
FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(8) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(9) Current for brownout included. Low-side supervisor and monitors disabled (SVS_L, SVM_L). High-side supervisor and monitor disabled (SVS_H, SVM_H). RAM retention enabled.

(10) $V_{VBAT} = V_{CC} – 0.2$ V, $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active

(11) $V_{VBAT} = V_{CC} – 0.2$ V, $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

(12) $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

8.6 Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREV	TEMPERATURE (T_A)								UNIT
				–40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM3}, LCD, ext. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, external biasing(1) (2)	3 V	0	3.7		4.3	4.9	5.5		9.0	15.0	µA
			1	4.1		4.7		5.9		9.6		
			2	4.5		5.1		6.3		10.2		
			3	4.5		5.2	5.8	6.5		10.4	18.0	
I_{LPM3}, LCD, int. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(1) (3)	3 V	0	4.2		4.8	5.4	6.0		9.6	17.0	µA
			1	4.7		5.4		6.6		10.4		
			2	5.1		5.8		7.1		11.0		
			3	5.0		5.7	6.4	7.0		11.0	19.0	
I_{LPM3} LCD,CP	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled(1) (4)	2.2 V	0			6.4						µA
			1			6.77						
			2			7.13						
		3 V	0			6.53						µA
			1			7.0						
			2			7.43						
			3			7.6						

(1) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz
Current for brownout included. Low-side supervisor (SVS_L) and low-side monitor (SVM_L) disabled. High-side supervisor (SVS_H) and high-side monitor (SVM_H) disabled. RAM retention enabled.

(2) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(3) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD} = 3$ V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

8.7 Thermal Resistance Characteristics

PARAMETER			VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air (1)	QFP (PZ)	122	°C/W
		BGA (ZQW)	108	
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance (2)	QFP (PZ)	83	°C/W
		BGA (ZQW)	72	
θ_{JB}	Junction-to-board thermal resistance (3)	QFP (PZ)	98	°C/W
		BGA (ZQW)	76	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

8.8 Timing and Switching Characteristics

8.8.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Absolute Maximum Ratings. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

Section 8.8.1.1 lists the device reset requirements.

8.8.1.1 Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC\_BOR\_IT-)}$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s			1.47	V
$V_{(DVCC\_BOR\_IT+)}$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s	0.80	1.30	1.55	V
$V_{(DVCC\_BOR\_hys)}$	BOR_H hysteresis		60		250	mV

8.8.2 Reset Timing

Section 8.8.2.1 lists the reset input timing.

8.8.2.1 Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TYP	UNIT
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset	2	µs

8.8.3 Clock Specifications

Section 8.8.3.1 lists the characteristics of XT1 in low-frequency mode.

8.8.3.1 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC,LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1	3 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2) (3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0(8)		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF
- For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le 9$ pF
- For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le 10$ pF
- For XT1DRIVEx = 3, $C_{L,ef\,f} \ge 6$ pF

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Section 8.8.3.2 lists the characteristics of XT2.

8.8.3.2 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 0	3 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 1			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 2			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 3			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency	XT2BYPASS = 1(3) (4)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Start-up time	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator, observe the following guidelines.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Section 8.8.3.3 lists the characteristics of the VLO.

8.8.3.3 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Section 8.8.3.4 lists the characteristics of the REFO.

8.8.3.4 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Section 8.8.3.5 lists the characteristics of the DCO frequency.

8.8.3.5 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz,		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

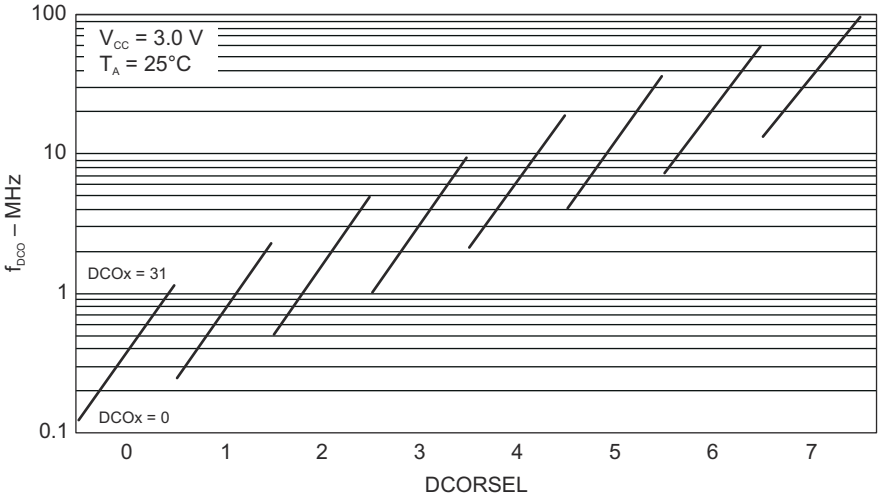


Figure 8-2. Typical DCO Frequency

8.8.4 Wake-up Characteristics

Section 8.8.4.1 lists the characteristics of the wake-up times.

8.8.4.1 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geq 4$ MHz		3	6.5	µs
			1 MHz < f_{MCLK} < 4 MHz		4	8.0	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(2) (3)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM3.5 or LPM4.5 to active mode(4)				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode(4)				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-FAST}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the MSP430F5xx and MSP430F6xx Family User's Guide.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-SLOW}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the MSP430F5xx and MSP430F6xx Family User's Guide.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.

8.8.5 General-Purpose I/Os

Section 8.8.5.1 lists the characteristics of the Schmitt-trigger inputs.

8.8.5.1 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) The same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Section 8.8.5.2 lists the characteristics of P1, P2, P3, and P4 .

8.8.5.2 Inputs – Ports P1, P2, P3, and P4

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing(2)	Port P1, P2, P3, P4: P1.x to P4.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Section 8.8.5.3 lists the leakage current of the GPIOs.

8.8.5.3 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	See (1) (2)	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Section 8.8.5.4 lists the output characteristics of the GPIOs.

8.8.5.4 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA(1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Section 8.8.5.5 lists the output characteristics of the GPIOs.

8.8.5.5 Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) Selecting reduced drive strength may reduce EMI.

Section 8.8.5.6 lists the frequency characteristics of the GPIOs.

8.8.5.6 Output Frequency – Ports P1, P2 and P3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P3.4/TA2CLK/SMCLK/S27 C_L = 20 pF, R_L = 1 kΩ(1) or 3.2 kΩ(2) (3)	V_{CC} = 1.8 V PMMCOREVx = 0		8	MHz
			V_{CC} = 3 V PMMCOREVx = 3		20	
f_{Port_CLK}	Clock output frequency	P1.0/TA0CLK/ACLK/S39 P3.4/TA2CLK/SMCLK/S27 P2.0/P2MAP0 (P2MAP0 = PM_MCLK) C_L = 20 pF(3)	V_{CC} = 1.8 V PMMCOREVx = 0		8	MHz
			V_{CC} = 3 V PMMCOREVx = 3		20	

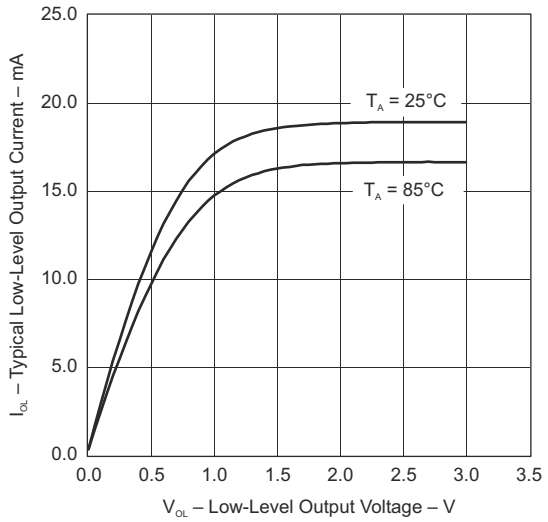
(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(3) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

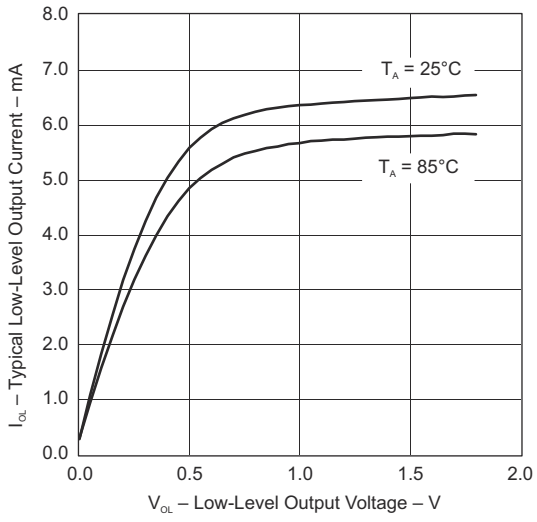
8.8.5.7 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



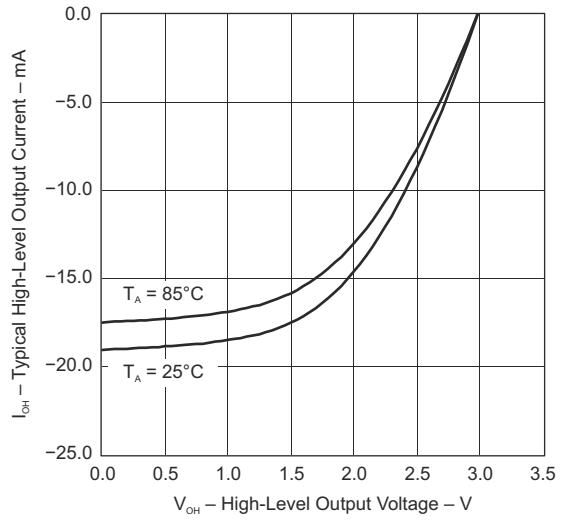
V_{CC} = 3.0 V P3.2

Figure 8-3. Typical Low-Level Output Current vs Low-Level Output Voltage



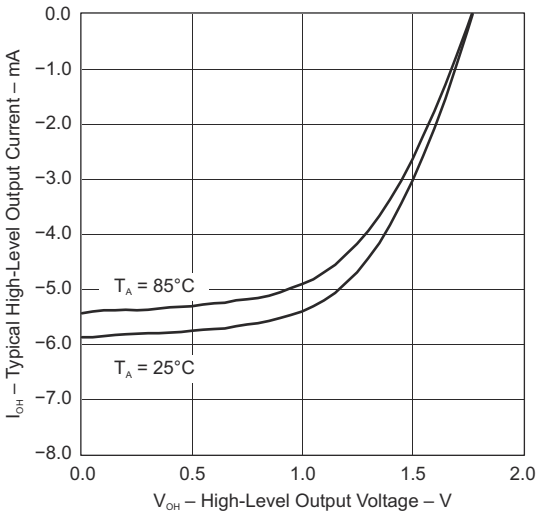
V_{CC} = 1.8 V P3.2

Figure 8-4. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.0 V P3.2

Figure 8-5. Typical High-Level Output Current Vs High-Level Output Voltage

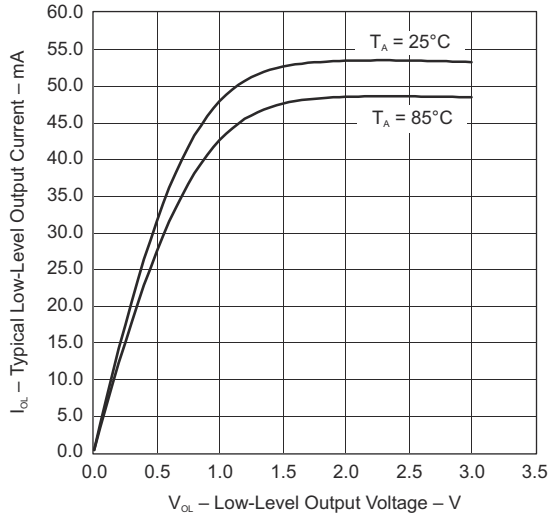


V_{CC} = 1.8 V P3.2

Figure 8-6. Typical High-Level Output Current Vs High-Level Output Voltage

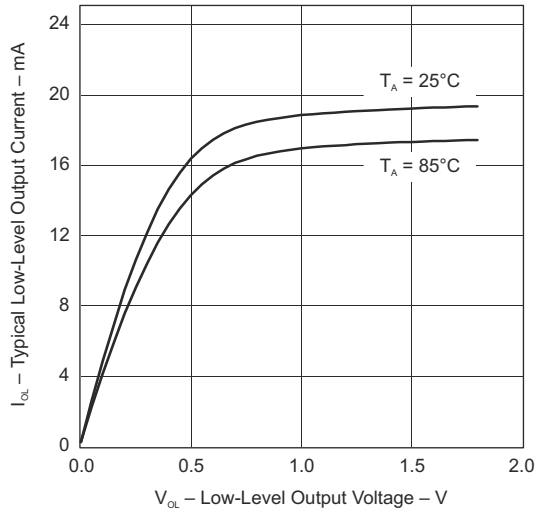
8.8.5.8 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



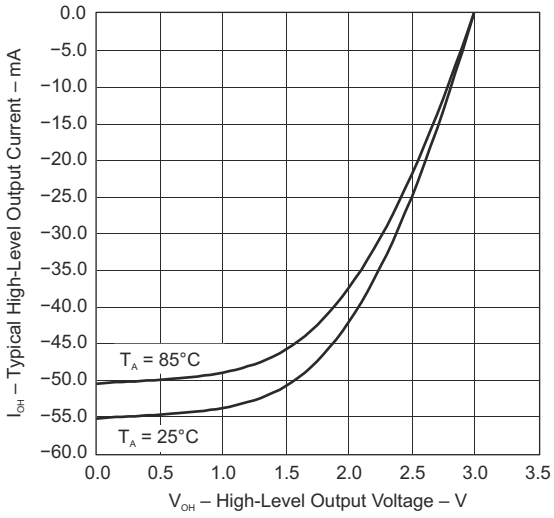
V_{CC} = 3.0 V P3.2

Figure 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage



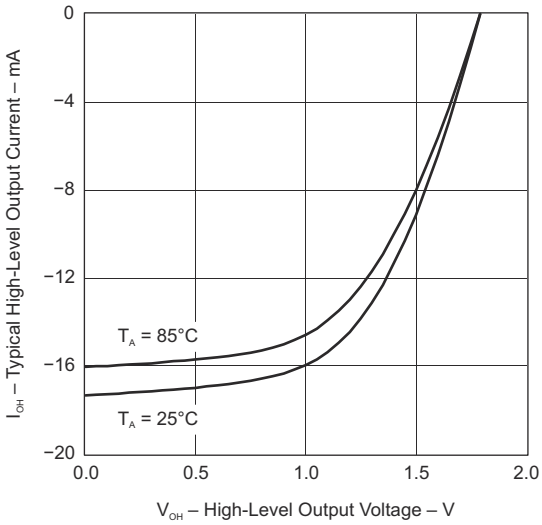
V_{CC} = 1.8 V P3.2

Figure 8-8. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.0 V P3.2

Figure 8-9. Typical High-Level Output Current vs High-level Output Voltage



V_{CC} = 1.8 V P3.2

Figure 8-10. Typical High-Level Output Current vs High-level Output Voltage

8.8.6 PMM

Section 8.8.6.1 lists the characteristics of the PMM core voltage.

8.8.6.1 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 17 mA		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 13 mA		1.40		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.44		V

Section 8.8.6.2 lists the characteristics of the SVS high side.

8.8.6.2 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		2.0		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.59	1.64	1.69	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.84	1.91	
		SVSHE = 1, SVSHRVL = 2	1.98	2.04	2.11	
		SVSHE = 1, SVSHRVL = 3	2.10	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.81	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.26	2.33	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVSHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0→1, SVSHFP = 1		12.5		µs
		SVSHE = 0→1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the MSP430F5xx and MSP430F6xx Family User's Guide on recommended settings and use.

Section 8.8.6.3 lists the characteristics of the SVM high side.

8.8.6.3 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		2.0		µA
$V_{(SVMH)}$	SVM_H on or off voltage level(1)	SVMHE = 1, SVSMHRRL = 0	1.65	1.74	1.86	V
		SVMHE = 1, SVSMHRRL = 1	1.85	1.94	2.02	
		SVMHE = 1, SVSMHRRL = 2	2.02	2.14	2.22	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.26	2.35	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVMHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0→1, SVSMFP = 1		12.5		µs
		SVMHE = 0→1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the MSP430F5xx and MSP430F6xx Family User's Guide on recommended settings and use.

Section 8.8.6.4 lists the characteristics of the SVS low side.

8.8.6.4 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0→1, SVSLFP = 1		12.5		µs
		SVSLE = 0→1, SVSLFP = 0		100		

Section 8.8.6.5 lists the characteristics of the SVM low side.

8.8.6.5 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		2.0		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0→1, SVMLFP = 1		12.5		µs
		SVMLE = 0→1, SVMLFP = 0		100		

8.8.7 Timers

Section 8.8.7.1 lists the characteristics of Timer_A.

8.8.7.1 Timer_A, Timers TA0, TA1, and TA2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		20	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

Section 8.8.7.2 lists the characteristics of Timer_B.

8.8.7.2 Timer_B, Timer TB0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V, 3 V		20	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

8.8.8 Battery Backup

Section 8.8.8.1 lists the characteristics of the battery backup.

8.8.8.1 Battery Backup

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_{VBAT}	Current into VBAT terminal in case no primary battery is connected.	VBAT = 1.7 V, DVCC not connected, RTC running	T_A = –40°C			0.43		µA
			T_A = 25°C			0.52		
			T_A = 60°C			0.58		
			T_A = 85°C			0.66		
		VBAT = 2.2 V, DVCC not connected, RTC running	T_A = –40°C			0.50		
			T_A = 25°C			0.59		
			T_A = 60°C			0.64		
			T_A = 85°C			0.72		
		VBAT = 3 V, DVCC not connected, RTC running	T_A = –40°C			0.68		
			T_A = 25°C			0.75		
			T_A = 60°C			0.79		
			T_A = 85°C			0.86		
V_{SWITCH}	Switch-over level (V_{CC} to VBAT)	C_{VCC} = 4.7 µF	General			V_{SVSH_IT-}		V
			SVSHRL = 0		1.59		1.69	
			SVSHRL = 1		1.79		1.91	
			SVSHRL = 2		1.98		2.11	
			SVSHRL = 3		2.10		2.23	
R_{ON_VBAT}	ON-resistance of switch between VBAT and VBAK	V_{BAT} = 1.8 V		0 V		0.35	1	kΩ
V_{BAT3}	VBAT to ADC: V_{BAT} divided, $V_{BAT3} = V_{BAT}$ /3			1.8 V		0.6	±5%	V
				3 V		1.0	±5%	
				3.6 V		1.2	±5%	
V_{CHVx}	Charger end voltage	CHVx = 2			2.65	2.7	2.9	V
R_{CHARGE}	Charge limiting resistor		CHCx = 1				5.2	kΩ
			CHCx = 2				10.2	
			CHCx = 3				20	

8.8.9 USCI

Section 8.8.9.1 lists the characteristics of the USCI in UART mode.

8.8.9.1 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)				1	MHz
t_T	UART receive deglitch time(1)		2.2 V	50	600	ns
			3 V	50	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Section 8.8.9.2 lists the characteristics of the USCI in SPI master mode.

8.8.9.2 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 8-11 and Figure 8-12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK, duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55		ns
			3 V	38		
		PMMCOREV = 3	2.4 V	30		
			3 V	25		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0		ns
			3 V	0		
		PMMCOREV = 3	2.4 V	0		
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		20	ns
			3 V		18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		16	
			3 V		15	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	–10		ns
			3 V	–8		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	–10		
			3 V	–8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-11 and Figure 8-12.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 8-11 and Figure 8-12.

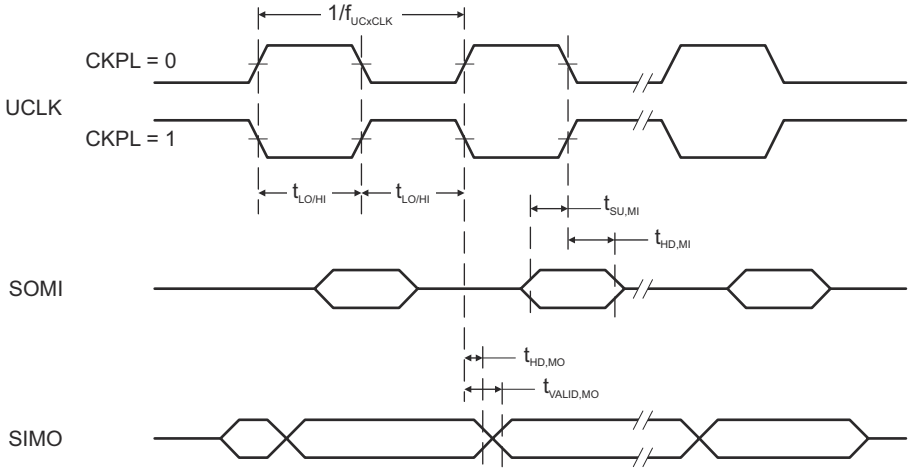


Figure 8-11. SPI Master Mode, CKPH = 0

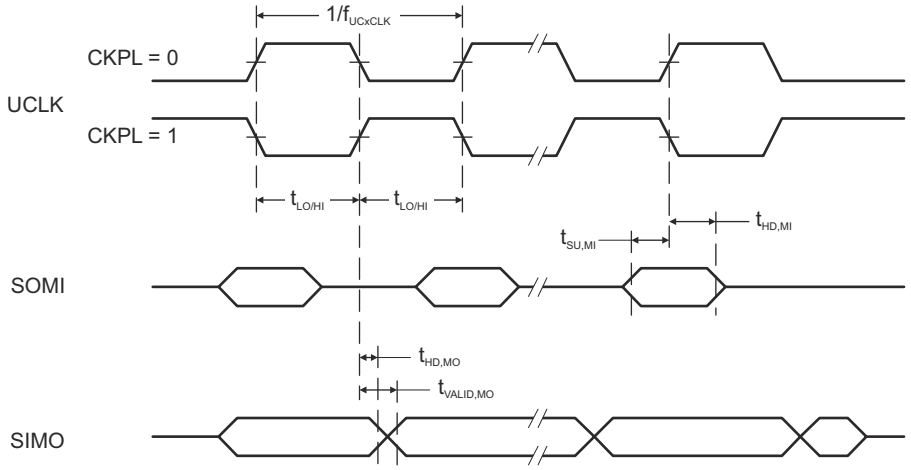


Figure 8-12. SPI Master Mode, CKPH = 1

Section 8.8.9.3 lists the characteristics of the USCI in SPI slave mode.

8.8.9.3 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 8-13 and Figure 8-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11		ns
			3 V	8		
		PMMCOREV = 3	2.4 V	7		
			3 V	6		
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3		ns
			3 V	3		
		PMMCOREV = 3	2.4 V	3		
			3 V	3		
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V		66	ns
			3 V		50	
		PMMCOREV = 3	2.4 V		36	
			3 V		30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V		30	ns
			3 V		30	
		PMMCOREV = 3	2.4 V		30	
			3 V		30	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	2		
			3 V	2		
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	5		
			3 V	5		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		76	ns
			3 V		60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		44	
			3 V		40	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	12		ns
			3 V	12		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	12		
			3 V	12		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-13 and Figure 8-14.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 8-13 and Figure 8-14.

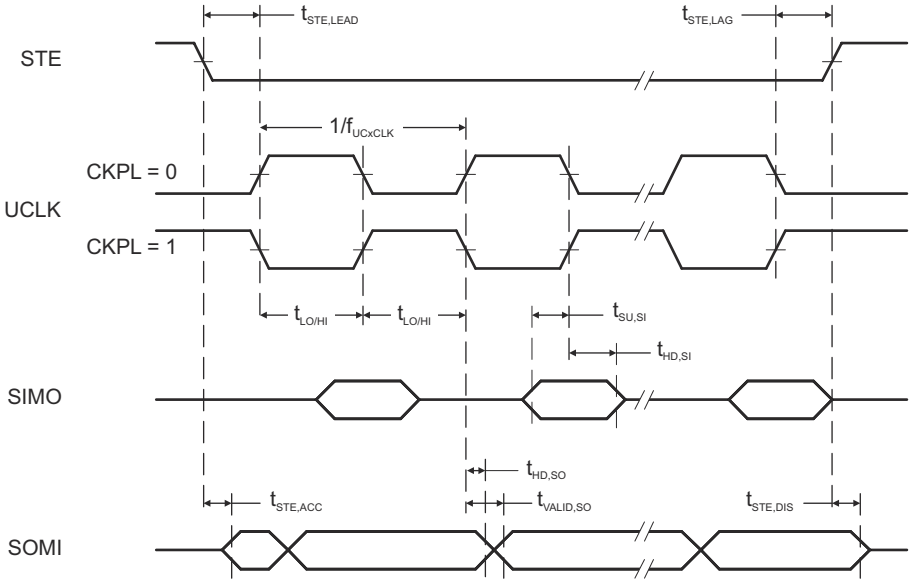


Figure 8-13. SPI Slave Mode, CKPH = 0

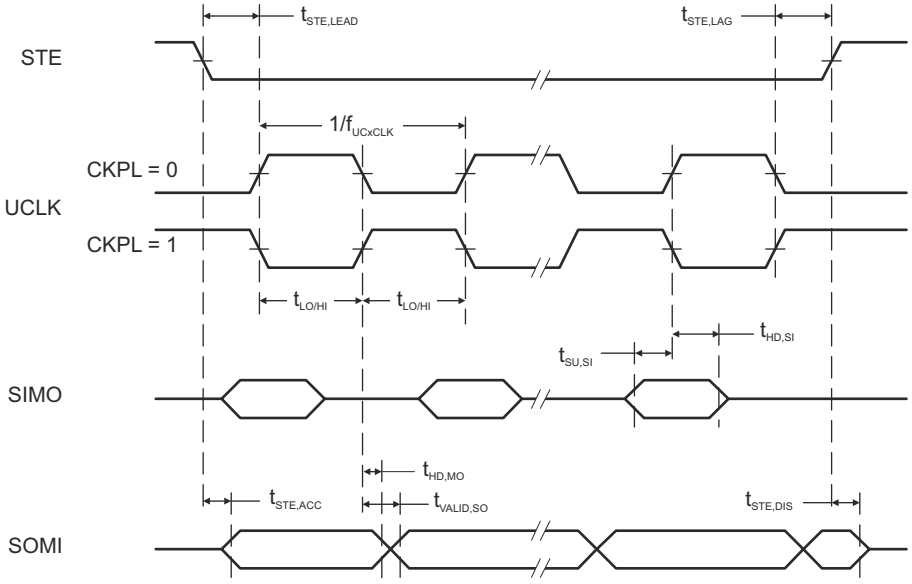


Figure 8-14. SPI Slave Mode, CKPH = 1

Section 8.8.9.4 lists the characteristics of the USCI in I²C mode.

8.8.9.4 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.0		µs
		$f_{SCL} > 100$ kHz		0.6		
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.7		µs
		$f_{SCL} > 100$ kHz		0.6		
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0		ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250		ns
$t_{SU,STO}$	Setup time for STOP	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.0		µs
		$f_{SCL} > 100$ kHz		0.6		
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
			3 V	50	600	

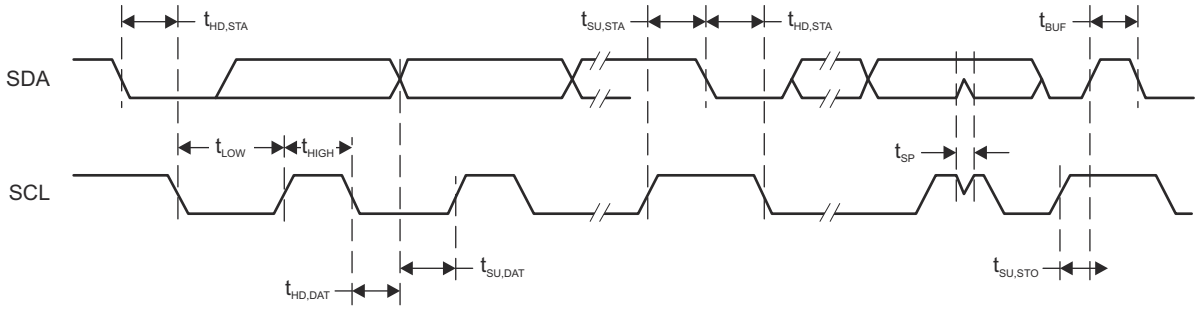


Figure 8-15. I²C Mode Timing

8.8.10 LCD Controller

Section 8.8.10.1 lists the operating conditions of the LCD controller.

8.8.10.1 LCD_B Operating Conditions

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD\_B,CP\ en,3.6}$	Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V	LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, $V_{LCD} \le 3.6$ V)	2.2		3.6	V
$V_{CC,LCD\_B,CP\ en,3.3}$	Supply voltage range, charge pump enabled, $V_{LCD} \le 3.3$ V	LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, $V_{LCD} \le 3.3$ V)	2.0		3.6	V
$V_{CC,LCD\_B,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD\_B,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD\_B,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.0		3.6	V
$V_{LCDCAP/R33}$	External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.4		3.6	V
C_{LCDCAP}	Capacitor on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000 (charge pump enabled)		4.7	10	µF
f_{Frame}	LCD frame frequency range	$f_{LCD} = 2 \times mux \times f_{FRAME}$ (mux = 1 (static), 2, 3, 4)	0		100	Hz
$f_{ACLK,in}$	ACLK input frequency range		30	32	40	kHz
C_{Panel}	Panel capacitance	100-Hz frame frequency			10000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT = 1	2.4		V_{CC} + 0.2	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	$V_{R03} + 2/3 \times (V_{R33} - V_{R03})$	V_{R33}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	$V_{R03} + 1/3 \times (V_{R33} - V_{R03})$	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1	V_{R03}	$V_{R03} + 1/2 \times (V_{R33} - V_{R03})$	V_{R33}	V
V_{R03}	Analog input voltage at R03	R0EXT = 1	V_{SS}			V
V_{LCD}-V_{R03}	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT = 1	2.4		V_{CC} + 0.2	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13	VLCDREFx = 01	0.8	1.2	1.5	V

Section 8.8.10.2 lists the characteristics of the LCD controller.

8.8.10.2 LCD_B, Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{LCD}	LCD voltage	VLCDx = 0000, VLCDEXT = 0	2.4 V to 3.6 V		V_{CC}		V
		LCDCPEN = 1, VLCDx = 0001	2 V to 3.6 V		2.60		
		LCDCPEN = 1, VLCDx = 0010	2 V to 3.6 V		2.66		
		LCDCPEN = 1, VLCDx = 0011	2 V to 3.6 V		2.72		
		LCDCPEN = 1, VLCDx = 0100	2 V to 3.6 V		2.79		
		LCDCPEN = 1, VLCDx = 0101	2 V to 3.6 V		2.85		
		LCDCPEN = 1, VLCDx = 0110	2 V to 3.6 V		2.92		
		LCDCPEN = 1, VLCDx = 0111	2 V to 3.6 V		2.98		
		LCDCPEN = 1, VLCDx = 1000	2 V to 3.6 V		3.05		
		LCDCPEN = 1, VLCDx = 1001	2 V to 3.6 V		3.10		
		LCDCPEN = 1, VLCDx = 1010	2 V to 3.6 V		3.17		
		LCDCPEN = 1, VLCDx = 1011	2 V to 3.6 V		3.24		
		LCDCPEN = 1, VLCDx = 1100	2 V to 3.6 V		3.30		
		LCDCPEN = 1, VLCDx = 1101	2.2 V to 3.6 V		3.36		
		LCDCPEN = 1, VLCDx = 1110	2.2 V to 3.6 V		3.42		
		LCDCPEN = 1, VLCDx = 1111	2.2 V to 3.6 V		3.48	3.6	
$I_{CC,Peak,CP}$	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111	2.2 V		400		µA
$t_{LCD,CP,on}$	Time to charge C_{LCD} when discharged	C_{LCD} = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111	2.2 V		100	500	ms
$I_{CP,Load}$	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111	2.2 V	50			µA
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

8.8.11 CTSD16

Note

The delta-sigma analog-to-digital converter uses the CTSD16. The CTSD16 is proceeded by a unity-gain buffer stage following the channel muxing as shown in Figure 9-2. See Section 8.8.14.1 for the electrical characteristics of the PGA buffer stages.

Section 8.8.11.1 lists the operating conditions of the CTSD16.

8.8.11.1 CTSD16, Power Supply and Operating Conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	AVSS = DVSS = 0 V			2.2		3.6	V
I_{CTSD16}	Analog plus digital supply current per converter (reference current not included)	CTSD16OSRx = 256, CTSD16RRI = 0	GAIN: 1, 2, 4, 8, 16	3 V		190(1)		µA
			GAIN: 1, 16	3 V			300(1)	
$I_{CTSD16CLK}$	CTSD16 clock current consumption	This is requested when CTSD16 is converting, or CTSD16RRIBURST = 0, or when OA is in rail-to-rail input mode (OARRI = 1), or when OA charge pump is on. The current should only be counted once even if both OA and CTSD16 are requesting the clock.		3 V		205	240	µA

(1) See Table 8-1 to calculate total current from CTSD16 for different use cases.

Table 8-1 explains how to compute the total current, I_{TOTAL}, when the CTSD, along with associated modules, are used. See Section 8.8.14.2 for a similar table for the OA. A "yes" means it must be included in computing I_{TOTAL}. Here is an example current calculation for CTS16D in rail-to-rail input mode (CTSD16RRI = 1) using the internal reference (CTSD16REFS = 1) and OA0 and OA1 enabled in rail-to-rail input modes, OARRI = 1.

As an example, assume that the application uses the CTS16D in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I_{TOTAL}, would be computed as follows:

$$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA} \quad (1)$$

Table 8-1. CTSD16, Current Calculation

USE CASE NAME	USE CASE DETAILS	I_{CTSD16}	$I_{CTSD16CLK}$ (1)	I_{CP} (2)	I_{REFBG} (3)	I_{REF} (4)
CTSD16		yes	yes	no	yes if CTSD16REFS = 1 no if CTSD16REFS = 0	yes
CTSD16 rail-to-rail inputs	CTSD16RRI = 1	yes	yes	yes	yes if CTSD16REFS = 1 no if CTSD16REFS = 0	yes

(1) Count this only once no matter how many modules use it. OA can also use this when rail-to-rail input is selected.
(2) Count this only once no matter how many modules use it. OA also uses this. This current is listed in Section 8.8.14.1.
(3) Count this only once no matter how many modules use it. DAC can use this as well as internal reference when it is available externally, REFOUT = 1. This current is listed in Section 8.8.12.1.
(4) Count this only once no matter how many modules use it. This current is listed in Section 8.8.14.1. If I_{REFBG} is used that includes I_{REF} current.

Section 8.8.11.2 lists the characteristics of the CTSD16 external voltage reference.

8.8.11.2 CTSD16, External Voltage Reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{VeREF+}	Input voltage range	CTSD16REFS = 0	3 V	1.0	1.2	1.5	V
I_{VeREF+}	Input current	CTSD16REFS = 0	3 V			50	nA

Section 8.8.11.3 lists the characteristics of the CTSD16 input range.

8.8.11.3 CTSD16, Input Range

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full-scale input voltage range	$V_{ID} = V_{I,A+} - V_{I,A-}$			$-V_R$/Gain		$+V_R$/Gain	V
$V_{I,FSR}$	Single-ended full-scale input voltage range	$V_{ID} = V_{I,A+} - V_R$ *negative input is tied to* V_R			$V_R - V_R$/Gain		$V_R + V_R$/Gain	V
V_{ID}	Differential input voltage range for specified performance(2)	CTSD16REFS = 1	CTSD16GAINx = 1			±928		mV
			CTSD16GAINx = 2			±464		
			CTSD16GAINx = 4			±232		
			CTSD16GAINx = 8			±116		
			CTSD16GAINx = 16			±58		
V_I	Single-ended input voltage range for specified performance				V_R – (0.8 × V_R/Gain)		V_R + (0.8 × V_R/Gain)	V
Z_I	Input impedance (pin Ax or ADx+ or ADx- to AVSS)	CTSD16GAINx = 1, 16		3 V		20		MΩ
Z_{ID}	Differential input impedance (pin ADx+ to pin ADx-)	CTSD16GAINx = 1, 16		3 V		35		MΩ
V_I	Absolute input voltage range				AVSS		V_{CC}	V
V_{IC}	Common-mode input voltage range				AVSS		V_{CC}	V

(1) All parameters pertain to each CTSD16 input.

(2) The full-scale range is defined by $V_{FSR+} = +V_R/GAIN$ and $V_{FSR-} = -V_R/GAIN$; FSR = $V_{FSR+} - V_{FSR-} = 2xV_R/GAIN$. If V_R is sourced externally, the analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}; that is, V_{ID} = 0.8 V_{FSR-} to 0.8 V_{FSR+}. If V_R is sourced internally, the given V_{ID} ranges apply.

Section 8.8.11.4 lists the performance characteristics of the CTSD16.

8.8.11.4 CTSD16, Performance

CTSD16OSRx = 256, CTSD164REFS = 1 (see Figure 8-16, Figure 8-17, and Figure 8-18)

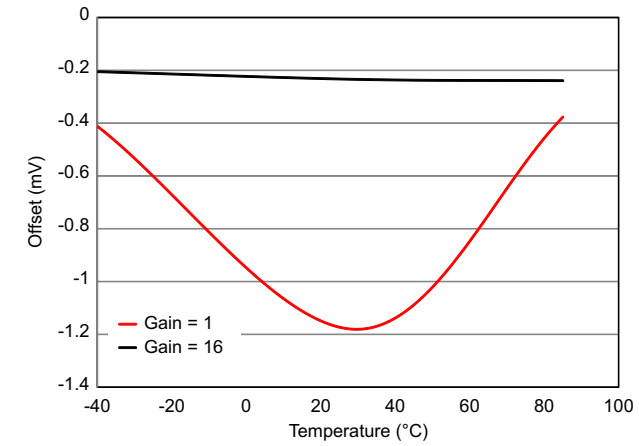
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
f_M	Modulator clock					1.024		MHz
SINAD	Signal-to-noise + distortion ratio for differential inputs	CTSD16GAINx = 1, input ADx+ and ADx- (differential)	f_{IN} = 50 Hz(1)	3 V	84	87		dB
		CTSD16GAINx = 2, input ADx+ and ADx- (differential)				86		
		CTSD16GAINx = 4, input ADx+ and ADx- (differential)				85		
		CTSD16GAINx = 8, input ADx+ and ADx- (differential)				82		
		CTSD16GAINx = 16, input ADx+ and ADx- (differential)				77		
SINAD	Signal-to-noise + distortion ratio for single-ended input	CTSD16GAINx = 1, input Ax (single-ended)	f_{IN} = 50 Hz(1)	3 V		83		dB
		CTSD16GAINx = 2, input Ax (single-ended)				82		
		CTSD16GAINx = 4, input Ax (single-ended)				78		
		CTSD16GAINx = 8, input Ax (single-ended)				72		
		CTSD16GAINx = 16, input Ax (single-ended)				66		
G	Nominal gain	CTSD16GAINx = 1		3 V		1		
		CTSD16GAINx = 2				2		
		CTSD16GAINx = 4				4		
		CTSD16GAINx = 8				8		
		CTSD16GAINx = 16				16		
E_G	Gain error	CTSD16GAINx: 1, 8, or 16 with external reference (1.2 V)		3 V	–1%		+1%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient, internal reference	CTSD16GAINx: 1, 8, or 16		3 V		3	50	ppm/°C
$\Delta E_G/\Delta T$	Gain error temperature coefficient, external reference	CTSD16GAIN: 1, 8, or 16 with external reference (1.2 V)		3 V		4	15	ppm/°C
$\Delta E_G/\Delta VCC$	Gain error vs VCC	CTSD16GAINx: 1, 8, or 16				0.02		%/V
E_{OS}	Offset error	CTSD16GAINx = 1		3 V			±4.1	mV
		CTSD16GAINx = 16					±3.4	
ΔEOS/ΔT	Offset error temperature coefficient	CTSD16GAINx = 1, 16		3 V		±1	±10	ppm FSR/°C
ΔEOS/ ΔVCC	Offset error vs VCC	CTSD16GAINx = 1, 16		3 V		11		µV/V
CMRR, 50Hz	Common-mode rejection ratio at 50 Hz	CTSD16GAINx = 1, V_{ID} = 928 mV, f_{IN} = 50 Hz		3 V		78		dB
		CTSD16GAINx = 16, V_{ID} = 58 mV, f_{IN} = 50 Hz				80		

8.8.11.4 CTSD16, Performance (continued)

CTSD16OSRx = 256, CTSD164REFS = 1 (see Figure 8-16, Figure 8-17, and Figure 8-18)

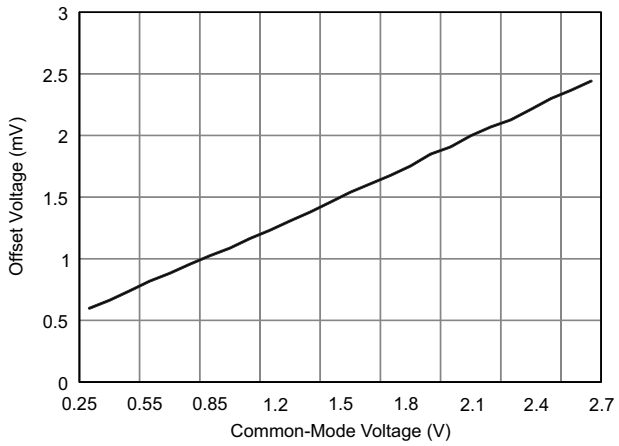
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AC PSRR	AC power supply rejection ratio	CTSD16GAINx: 1, V_{CC} = 3 V ±50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz, Inputs grounded (no analog signal applied)			95		dB
		CTSD16GAINx: 8, V_{CC} = 3 V ±50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz, Inputs grounded (no analog signal applied)			105		
		CTSD16GAINx: 16, V_{CC} = 3 V ±50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz, Inputs grounded (no analog signal applied)			105		
DC PSRR	DC power supply rejection ratio	CTSD16GAINx: (1, 8, 16), V_{CC} = 2.2 V to 3.6 V, (PSRR [dB] = –20 log(dVout/dVcc) with dVout observed as change in the digital conversion result; assumed to be dominated by reference)			90		dB

(1) The following voltages were applied to the CTSD16 inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A–}(t) = 0\ V – V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{IN,A+}(t) – V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to CTSD16 input range).



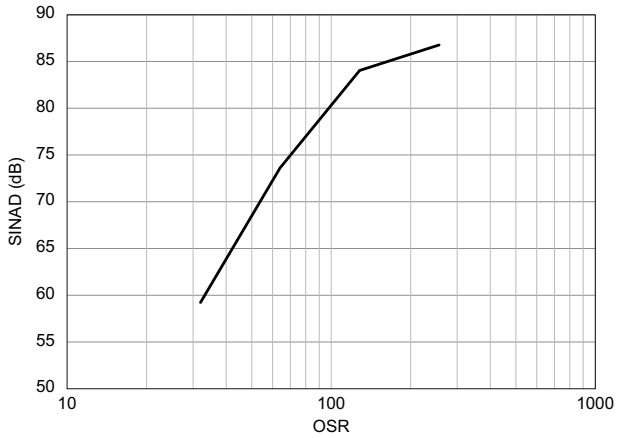
A. Average of four typical devices

Figure 8-16. CTSD16 Offset Voltage vs Temperature



A. Gain = 1 OSR = 256 DIfferential Signal = 300

Figure 8-17. CTSD16 Typical Offset Voltage vs Common-Mode Voltage



CTSD16REFS = 1 CTSD16GAINx = 1

Figure 8-18. SINAD Performance vs OSR

Section 8.8.11.5 lists the characteristics of the built-in V_{cc} sense.

8.8.11.5 Built-in V_{cc} Sense

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC,sense}$	AV_{CC} divider	CTSD16ON = 1, CTSD16INCH = 0111	0.95 × (AVCC / 2)	AVCC / 2	1.05 × (AVCC / 2)	V

Section 8.8.11.6 lists the characteristics of the temperature sensor.

8.8.11.6 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{sensor}	Temperature sensor output voltage(1) (2)	CTSD16ON = 1, CTSD16INCH = 110, V_{CC} = 3 V, T_A = 30°C		800		mV
I_{sensor}	Temperature sensor quiescent current consumption	CTSD16ON = 1, CTSD16INCH = 110, T_A = 85°C		2		uA

(1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.

(2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} * (Temperature, °C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.

8.8.12 REF

Section 8.8.12.1 lists the characteristics of the REF and REFBG built-in reference.

8.8.12.1 REF and REFBG, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{REFBG}	Operating supply current into AVCC terminal(1)	V_{CC} = 3.0 V, REFON = 1 and REFOUT = 1		110	130	µA
V_{REFBG}	Bandgap output voltage calibrated	V_{CC} = 3.0 V, VeREF+ ≤ 1.5 V if used	1.146	1.16	1.174	V
I_{REF}	Operating supply current into AVCC terminal(1)	V_{CC} = 3.0 V, REFON = 1		15	20	µA
V_{REF}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1		2.5	±1%	V
		REFVSEL = {1} for 2.0 V, REFON = 1		2.0	±1%	
		REFVSEL = {0} for 1.5 V, REFON = 1		1.5	±1%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	DAC12SREFx = 0, REFVSEL = {0} for 1.5 V	2.2			V
		DAC12SREFx = 0, REFVSEL = {1} for 2 V	2.3			
		DAC12SREFx = 0, REFVSEL = {2} for 2.5 V	2.8			
PSRR_DC	Power supply rejection ratio (DC)	V_{CC} = 2.2 V to 3.6 V, T_A = 25°C		50		µV/V
PSRR_AC	Power supply rejection ratio (AC)	V_{CC} = 2.2 V to 3.6 V, T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV		1.5		mV/V
TC_{REF+}	Bandgap reference temperature coefficient(2)	I_{VREF+} = 0 A		15	50	ppm/°C
t_{SETTLE}	Settling time of V_{REFBG} reference voltage(3)	AV_{CC} = $AV_{CC\ (min)}$ through $AV_{CC(max)}$, REFON = 0 → 1			120	µs
C_{VREFBG}	Capacitance at VREFBG terminal	See (4)			1	nF
I_{LOAD}	VREFBG maximum load current	REFOUT = REFON = 1			1	mA
$I_{L(VREFBG)}$	Load-current regulation, VREFBG terminal(5)	$I_{(VREF+)}$ = +1 mA or –1 mA, AV_{CC} = $AV_{CC\ (min)}$, REFON = REFOUT = 1			3.5	mV/mA

(1) The internal reference current is supplied from terminal AVCC. Consumption is independent of the CTSD16ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).

(3) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

(4) There is no capacitance required on VREFBG if the reference voltage is not used externally. However, TI recommends a capacitance close to the maximum value to reduce any reference voltage noise.

(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB traces or other external factors.

8.8.13 DAC

Section 8.8.13.1 lists the supply specifications of the DAC.

8.8.13.1 12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} = 0 V		2.2		3.6	V
I_{DD}	Supply current, single DAC channel(1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12OG = 1, DAC12_xDAT = 0800h, VeREF+ = VREFBG = 1.16 V	3 V		65	110	µA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV_{CC}	2.2 V to 3.6 V		125	165	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV_{CC}			250	350	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV_{CC}			750	1100	
PSRR	Power supply rejection ratio(3) (4)	DAC12_xDAT = 800h, VeREF+ = 1.16 V or 1.5 V, ΔAV_{CC} = 100 mV	2.2 V to 3.6 V		70		dB
		DAC12_xDAT = 800h, VeREF+ = 1.16 V or 2.5 V ΔAV_{CC} = 100 mV	3 V		70		

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications Section 8.8.13.4.
(3) PSRR = 20 log (ΔAV_{CC} / ΔV_{DAC12_xOUT})
(4) The internal reference is not used.

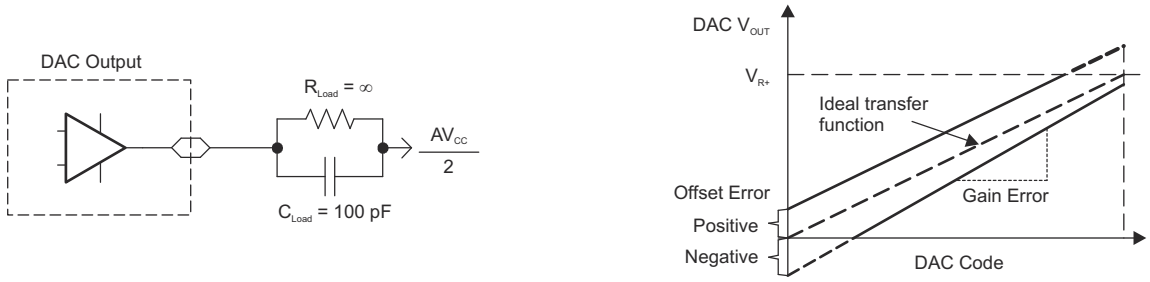


Figure 8-19. Linearity Test Load Conditions, Gain and Offset Definition

Section 8.8.13.2 lists the linearity specifications of the DAC.

8.8.13.2 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-19)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic			12			bits
INL	Integral nonlinearity(1)	V_{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1		2.2 V, 3 V		±2	±4	LSB
		V_{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1		2.2 V, 3 V		±2	±4	
DNL	Differential nonlinearity(1)	V_{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1		2.2 V, 3 V		±0.4	±1	LSB
		V_{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1		2.2 V, 3 V		±0.4	±1	
E_O	Offset voltage	Without calibration(1) (2)	V_{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V, 3 V			±21	mV
			V_{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V, 3 V			±21	
		With calibration(1) (2)	V_{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V, 3 V			±1.5	
			V_{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V, 3 V			±1.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient(1)	With calibration		2.2 V, 3 V		±10		µV/°C
E_G	Gain error	V_{eREF+} = 1.16 V		2.2 V, 3 V			±2.5	%FSR
		V_{eREF+} = 2.5 V		2.2 V, 3 V			±2.5	
$d_{E(G)}/d_T$	Gain temperature coefficient(1)			2.2 V, 3 V		10		ppm of FSR/ °C
t_{Offset_Cal}	Time for offset calibration(3)	DAC12AMPx = 2		2.2 V, 3 V			165	ms
		DAC12AMPx = 3, 5					66	
		DAC12AMPx = 4, 6, 7					16.5	

(1) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + bx. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (Ve_{REF+}/4095) \times DAC12\_xDAT$, DAC12IR = 1.

(2) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON

(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends configuring the DAC12 module before initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

Section 8.8.13.3 lists the output specifications of the DAC.

8.8.13.3 12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range[1] (see Figure 8-20)	No load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3.6 V	0		0.005	V
		No load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3.6 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current	DAC12AMPx = 2, DAC12_xDAT = 0FFFh, $V_{O/P(DAC12)} > AV_{CC}$ – 0.3	2.2 V, 3.6 V	–1			mA
		DAC12AMPx = 2, DAC12_xDAT = 0h, $V_{O/P(DAC12)}$ < 0.3 V				1	
$R_{O/P(DAC12)}$	Output resistance (see Figure 8-20)	R_{Load} = 3 kΩ, $V_{O/P}$(DAC12) < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V, 3.6 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$ – 0.3 V, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)} \le AV_{CC}$ – 0.3 V				6	

(1) Data is valid after the offset calibration of the output amplifier.

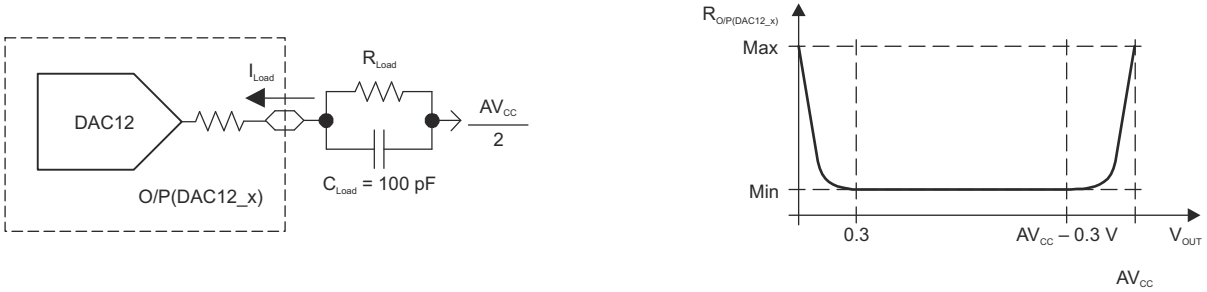


Figure 8-20. DAC12_x Output Resistance Tests

Section 8.8.13.4 lists the reference input specificaitons of the DAC.

8.8.13.4 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Reference input voltage range	DAC12IR = 0(1) (2)	2.2 V to 3.6 V		AV_{CC} / 3	AV_{CC} + 0.2	V
		DAC12IR = 1(3) (4)			AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREFBG)}$, $Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 DAC12IR = DAC12_1 DAC12IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 DAC12IR = 1, DAC12_1 DAC12IR = 0			52		kΩ
		DAC12_0 DAC12IR = 0, DAC12_1 DAC12IR = 1			52		
		DAC12_0 DAC12IR = DAC12_1 DAC12IR = 1, DAC12_0 DAC12SREFx = DAC12_1 DAC12SREFx(5)			26		

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AVCC).
(2) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AVCC).
(4) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel and reduce the reference input resistance.

Section 8.8.13.5 and Section 8.8.13.6 list the dynamic specifications of the DAC.

8.8.13.5 12-Bit DAC, Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see Figure 8-21 and Figure 8-22), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB(1) (see Figure 8-21)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h, BF8h → C08h → BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate	DAC12_xDAT = 80h → F7Fh → 80h(2)	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.35		V/µs
			DAC12AMPx = 3, 5		0.35	1.10		
			DAC12AMPx = 4, 6, 7		1.50	5.20		
	Glitch energy	DAC12_xDAT = 800h → 7FFh → 800h	DAC12AMPx = 7	2.2 V, 3 V		35		nV-s

(1) R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 8-21.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

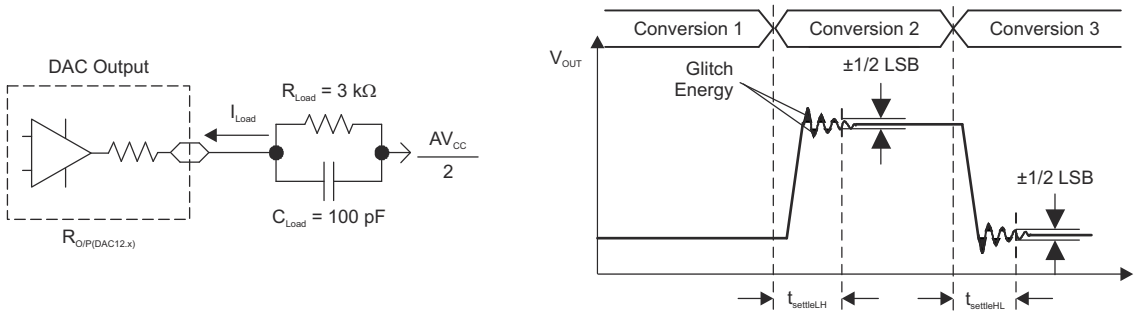


Figure 8-21. Settling Time and Glitch Energy Testing

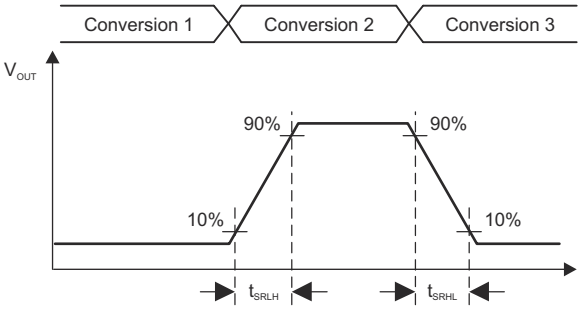


Figure 8-22. Slew Rate Testing

8.8.13.6 12-Bit DAC, Dynamic Specifications (Continued)

over recommended ranges of supply voltage and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 8-23)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			
	Channel-to-channel crosstalk(1) (see Figure 8-24)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz at 50/50 duty cycle	2.2 V, 3 V		–80		dB
		DAC12_0DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f_{DAC12_0OUT} = 10 kHz at 50/50 duty cycle			–80		

(1) R_{Load} = 3 kΩ, C_{Load} = 100 pF

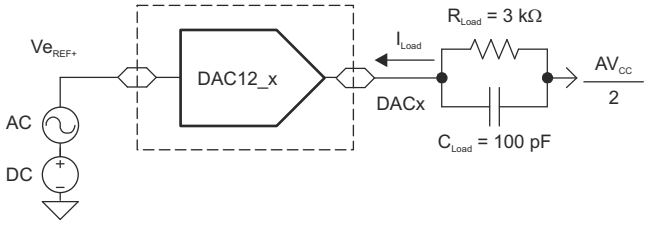


Figure 8-23. Test Conditions for 3-dB Bandwidth Specification

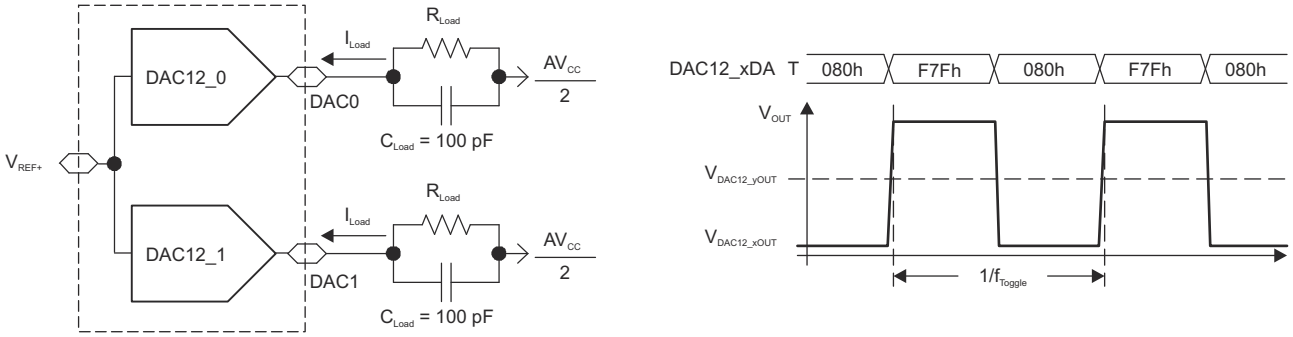


Figure 8-24. Crosstalk Test Conditions

8.8.14 Operational Amplifier

Section 8.8.14.1 lists the characteristics of the OA.

8.8.14.1 Operational Amplifier, OA0, OA1, PGA Buffers

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.2		3.6	V
C_{CPCAP}	External charge pump capacitor to AVSS.	Required when charge pump is enabled		20	22	24	nF
I_{CP_PEAK}	Charge pump peak current	OARRI = 0h to 1h, I_{CP_LOAD} = 0 µA			1.6		mA
I_{CP}	Charge pump average current	OARRI = 1h, I_{CP_LOAD} = 100 µA			570(1)	710(1)	µA
$t_{CP\_EN\_fast}$	Charge pump enable time fast	OARRI = 0h to 1h, I_{CP_LOAD} = 0 µA, AFE biases previously enabled and settled which can be done with REFON=1 or other modules requesting REFON.			50		µs
$t_{CP\_EN\_slow}$	Charge pump enable time slow	OARRI = 0h to 1h, I_{CP_LOAD} = 0 µA, Includes AFE bias settling			75		µs
I_{OA}	Supply current, per opamp	I_O = 0 mA, OARRI = 0h (charge pump disabled)			105(1)	130(1)	µA
V_{OS}	Input offset voltage	Noninverting, unity gain			±2		mV
dV_{OS}/dT	Input offset voltage temperature drift	Noninverting, unity gain			±1		µV/°C
dV_{OS}/dV	Input offset voltage voltage drift	Noninverting, unity gain			±3		µV/V
C_{in}	Input capacitance	Differential			4		pF
		Common mode			6		pF
PSRR_DC	Power supply rejection ratio, DC	Noninverting, unity gain, V_{INP} = positive input of OA = 1 V			50		µV/V
V_{CM}	Common mode voltage range(2)	OARRI = 0h, Noninverting, unity gain		0.1		V_{CC} - 1.0	V
		OARRI = 1h, Noninverting, unity gain		0.1		V_{CC} - 0.1	V
CMRR_DC	Common mode rejection ratio, DC	Over common-mode voltage range			110		dB
e_n	Input voltage noise density	f = 100 Hz, OARRI = 0h or 1h	3.0 V		90		nV/√Hz
		f = 50 kHz, OARRI = 0h or 1h	3.0 V		25		
A_{OL}	Open-loop voltage gain, DC				95		dB

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
GBW	Gain-bandwidth product	C_L = 100 pF, OAM = 1h			800		kHz
SR	Slew rate	Noninverting, unity gain, C_L = 100 pF, OAM = 1h			0.4		V/µs
t_{SETTLE}	Settling time	Noninverting, unity gain, 2.0-V step, 0.1%, OAM = 1h	3.0 V		5.3		µs
V_O	Voltage output swing from rail	–250 µA ≤ I_O ≤ 250 µA, Noninverting, unity gain (OAM = 1h)			5	55	mV
t_{EN_FAST}	Enable time fast	Noninverting, unity gain, OAM = 0h transition to 1h, AFE biases previously enabled and settled which can be done with REFON = 1 or other modules requesting REFON(3)			3	7	µs
t_{EN_SLOW}	Enable time slow	Noninverting,unity gain, OARRI = 0h transition to 1h, OAM = 0h transition to 1h, Includes AFE bias and charge pump settling(3)			190	225	µs
t_{DIS}	Disable time				0.4		µs

(1) See Section 8.8.14.2 to calculate total current from OA for different use cases.

(2) The common-mode input range is measured with the OA in a unity-gain source-follower configuration. The input signal is swept from 0 V to V_{CC}, and the output of the OA is monitored. The minimum and maximum values represent when the input and output differ more than 10 mV, not including the offset, V_{OS}.

(3) The AFE bias is used by several modules including the OA charge pump, OA, and CTSD16. Any of these modules will request the AFE bias when enabled. The AFE bias is generated by the REF module, so enabling the REF module also enables the AFE bias.

Section 8.8.14.2 explains how to compute the total current, I_{TOTAL}, when the OA and associated modules are used. See Table 8-1 for a similar table for the CTSD16. A "yes" means it must be included in computing I_{TOTAL}.

As an example, assume that the application uses the CTS16D in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I_{TOTAL}, would be computed as follows:

$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA}$

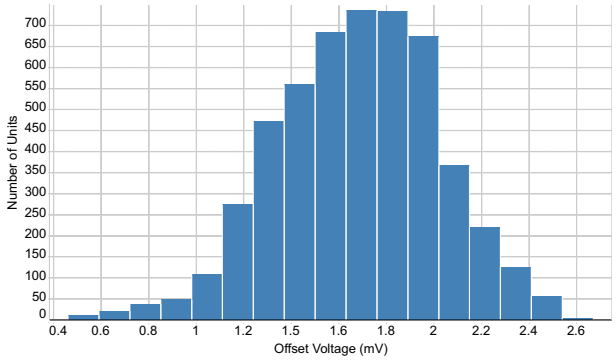


Figure 8-25. OA Offset Voltage Sample Production Distribution

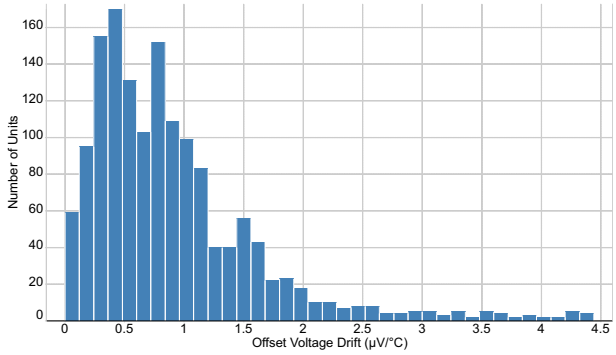


Figure 8-26. OA Offset Voltage Drift Sample Production Distribution

8.8.14.2 OA, Current Calculation

USE CASE NAME	USE CASE DETAILS	I_{OA}	$I_{CTSD16CLK}$ (1)	I_{CP} (2)	I_{REF} (3)
OA	OARRI = 0	yes	no	no	yes
OA with rail-to-rail input	OARRI = 1	yes	yes	yes	yes
Rail-to-rail input up, module off	(CTSD16SC = 0) AND (CTSD16RRI = 1) AND (CTSD16RRIBURST = 0) OR ((OARRI = 1 (for any OA)) AND (OAM = 0))	no	yes	yes	yes

(1) Count this current only once no matter how many modules use it. CTSD16 and the charge pump also use this. This current is listed in Section 8.8.11.1.
(2) Count this current only once no matter how many modules use it. CTSD16 also uses this when rail-to-rail inputs are selected.
(3) Count this current only once no matter how many modules use it. This current is listed in Section 8.8.14.1. If I_{REFBG} is used, that includes the I_{REF} current.

8.8.15 Switches

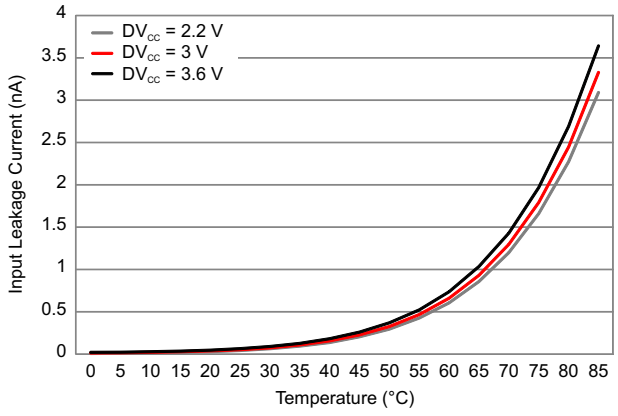
Section 8.8.15.1 lists the characteristics of the ground switches.

8.8.15.1 Ground Switches (GSW0A, GSW0B, GSW1A, GSW1B)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.2		3.6	V
I_{LKG}	Input leakage(1)	T_A = 0°C to 60°C		±0.25		nA
		T_A = –40°C to 85°C			±50	
I_{IN}	Input current switch to AVSS		0		100	µA
R_{ON}	Switch ON resistance with switch closed	I_{IN} = 100 µA, T_A = –40°C to 85°C		9.5	18.5	Ω
R_{OFF}	Switch OFF resistance with switch open	T_A = –40°C to 85°C, Input signal frequency < 100 Hz	100			MΩ
$t_{ON/OFF}$	Enable or disable time	T_A = –40°C to 85°C		0.25		µs

(1) Ground switches are shared with general-purpose I/Os. This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself.



Average of three typical devices

Figure 8-27. Ground Switch Input Leakage Current vs Temperature

Section 8.8.15.2 lists the characteristics of the OA switches.

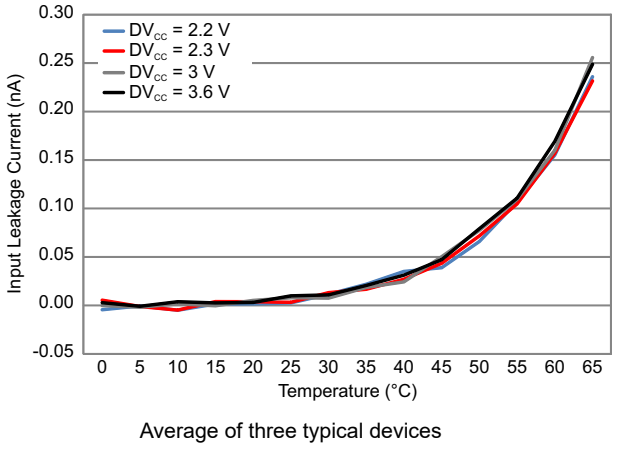
8.8.15.2 Operational Amplifier Switches

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.2		3.6	V
I_{LKG}	Input leakage[1]	T_A = 0°C to 60°C		±0.25		nA
		T_A = –40°C to 85°C			±50	
I_{IN}	Input current through switch		0		100	µA
R_{ON}	Switch ON resistance with switch closed[2]	I_{IN} = 100 µA, T_A = –40°C to 85°C		1		kΩ
R_{OFF}	Switch OFF resistance with switch open	T_A = –40°C to 85°C, Input signal frequency < 100 Hz	100			MΩ
$t_{ON/OFF}$	Enable or disable time	T_A = –40°C to 85°C		0.45		µs

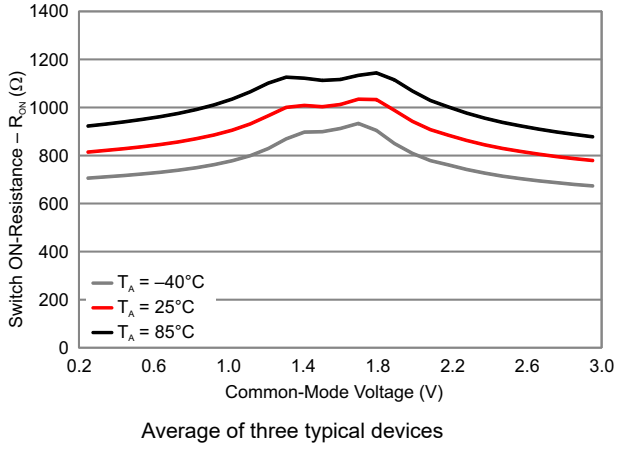
(1) This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself. It assumes a total of five switches present and a shared digital I/O.

(2) The resistance varies with input voltage range. This resistance represents the peak resistance at the worst case input range (see Figure 8-29).



Average of three typical devices

Figure 8-28. OA Switch Input Leakage Current vs Temperature



Average of three typical devices

Figure 8-29. OA Switch R_{ON} vs Common-Mode Voltage

8.8.16 Comparator

Section 8.8.16.1 lists the characteristics of the comparator.

8.8.16.1 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRSx = 00	1.8 V			40	µA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01, CBON = 1, CBRSx = 00	2.2 V, 3 V		10	30	
		CBPWRMD = 10, CBON = 1, CBRSx = 00	2.2 V, 3 V		0.5	1.3	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF module current	CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		10	22	µA
V_{IC}	Common mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00		–20		20	mV
		CBPWRMD = 01 or 10		–10		10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.5	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t_{EN_CMP}	Comparator enable time	CBON = 0 → 1, CBPWRMD = 00 or 01			1	2	µs
		CBON = 0 → 1, CBPWRMD = 10				100	
t_{EN_REF}	Resistor reference enable time	CBON = 0 → 1			1.0	1.5	µs
TC_{CB_REF}	Temperature coefficient of V_{CB_REF}					50	ppm/°C
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

8.8.17 USB

Section 8.8.17.1 lists the characteristics of PU.0 and PU.1.

8.8.17.1 Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (see Figure 8-31)	V_{USB} = 3.3 V ±10%, I_{OH} = –25 mA	2.4		V
V_{OL}	Low-level output voltage (see Figure 8-30)	V_{USB} = 3.3 V ±10%, I_{OL} = 25 mA		0.4	V
V_{IH}	High-level input voltage (see Figure 8-32)	V_{USB} = 3.3 V ±10%	2.0		V
V_{IL}	Low-level input voltage (see Figure 8-32)	V_{USB} = 3.3 V ±10%		0.8	V

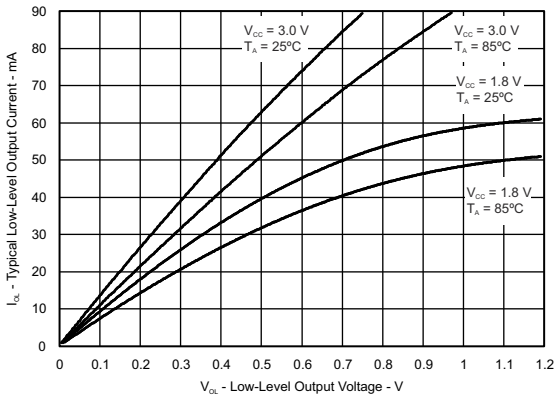


Figure 8-30. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

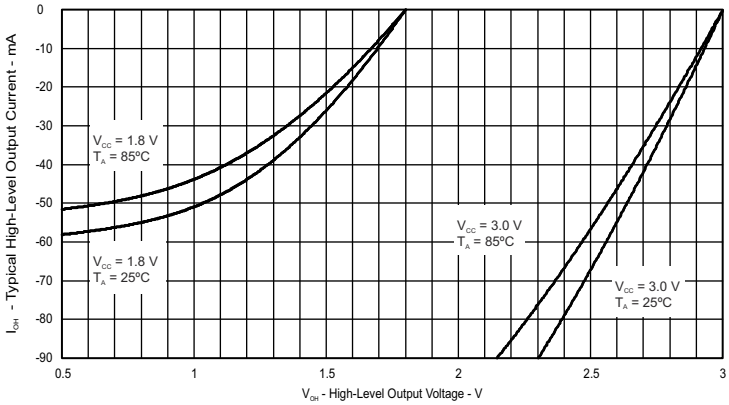


Figure 8-31. Ports PU.0, PU.1 Typical High-Level Output Characteristics

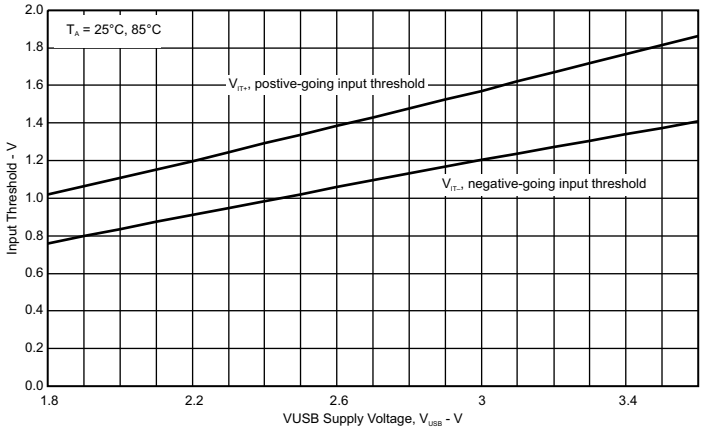


Figure 8-32. Ports PU.0, PU.1 Typical Input Threshold Characteristics

Section 8.8.17.2 and Section 8.8.17.3 list the characteristics of the DP and DM ports.

8.8.17.2 USB Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single ended	USB 2.0 load conditions	0	0.3	V
$Z_{(DRV)}$	D+, D– impedance	Including external series resistor of 27 Ω	28	44	Ω
t_{RISE}	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_{FALL}	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

8.8.17.3 USB Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$V_{(CM)}$	Differential input common mode range	0.8	2.5	V
$Z_{(IN)}$	Input impedance	300		kΩ
V_{CRS}	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic low level	0.8		V
V_{IH}	Static SE input logic high level		2.0	V
VDI	Differential input voltage		0.2	V

Section 8.8.17.4 lists the characteristics of the USB power system.

8.8.17.4 USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LAUNCH}	V_{BUS} detection threshold				3.75	V
V_{BUS}	USB bus voltage	Normal operation	3.76		5.5	V
V_{USB}	USB LDO output voltage			3.3	±9%	V
V_{18}	Internal USB voltage(1)			1.8		V
I_{USB_EXT}	Maximum external current from VUSB terminal(2)	USB LDO is on			12	mA
I_{DET}	USB LDO current overload detection(3)		60		100	mA
$I_{SUSPEND}$	Operating supply current into VBUS terminal(4)	USB LDO is on, USB PLL disabled			250	µA
C_{BUS}	VBUS terminal recommended capacitance			4.7		µF
C_{USB}	VUSB terminal recommended capacitance			220		nF
C_{18}	V18 terminal recommended capacitance			220		nF
t_{ENABLE}	Settling time V_{USB} and V_{18}	Within 2%, recommended capacitances			2	ms
RPUR	Pullup resistance of PUR terminal		70	110	150	Ω

(1) This voltage is for internal use only. No external DC loading should be applied.
(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.
(3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.
(4) Does not include current contribution of Rpu and Rpd as outlined in the USB specification.

Section 8.8.17.5 lists the characteristics of the USB PLL.

8.8.17.5 USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
I_{PLL}	Operating supply current			7	mA
f_{PLL}	PLL frequency		48		MHz
f_{UPD}	PLL reference frequency	1.5		3	MHz
t_{LOCK}	PLL lock time			2	ms
t_{Jitter}	PLL jitter		1000		ps

8.8.18 LDO-PWR (LDO Power System)

Section 8.8.18.1 lists the characteristics of the LDP power system.

8.8.18.1 LDO-PWR (LDO Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LAUNCH}	LDO input detection threshold				3.75	V
V_{LDOI}	LDO input voltage		3.76		5.5	V
V_{LDO}	LDO output voltage			3.3	±9%	V
V_{LDO_EXT}	LDOO terminal input voltage with LDO disabled	LDO disabled	1.8		3.6	V
I_{LDOO}	Maximum external current from LDOO terminal	LDO is on			20	mA
I_{DET}	LDO current overload detection (1)		60		100	mA
C_{LDOI}	LDOI terminal recommended capacitance			4.7		µF
C_{LDOO}	LDOO terminal recommended capacitance			220		nF
t_{ENABLE}	Settling time V_{LDO}	Within 2%, recommended capacitances			2	ms

(1) A current overload will be detected when the total current supplied from the LDO exceeds this value.

8.8.19 Flash

Section 8.8.19.1 lists the characteristics of the flash memory.

8.8.19.1 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_J	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DV_{CC} during program			3	5	mA
I_{ERASE}	Average supply current from DV_{CC} during erase			6	15	mA
I_{MERASE}, I_{BANK}	Average supply current from DV_{CC} during mass erase or bank erase			6	15	mA
t_{CPT}	Cumulative program time(1)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	25°C	100			years
t_{Word}	Word or byte program time(2)		64		85	µs
$t_{Block, 0}$	Block program time for first byte or word(2)		49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word(2)		37		49	µs
$t_{Block, N}$	Block program time for last byte or word(2)		55		73	µs
$t_{Seg Erase}$	Erase time for segment, mass erase, and bank erase when available(2)		23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

8.8.20 Debug and Emulation

Section 8.8.20.1 lists the characteristics of the JTAG and SBW interface.

8.8.20.1 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency (4-wire JTAG)(2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

9 Detailed Description

9.1 Overview

The MSP430FG6626 and MSP430FG6625 are microcontroller configurations with a high-performance 16-bit ADC, dual 12-bit DACs, dual low-power operational amplifiers, a comparator (COMPB), two USCIs, USB 2.0, a hardware multiplier (MPY32), DMA, four 16-bit timers, an RTC module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

The MSP430FG6426 and MSP430FG6425 are microcontroller configurations with a high-performance 16-bit ADC, dual 12-bit DACs, dual low-power operational amplifiers, a comparator (COMPB), two USCIs, a 3.3-V LDO, a hardware multiplier (MPY32), DMA, four 16-bit timers, an RTC module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

9.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 9-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

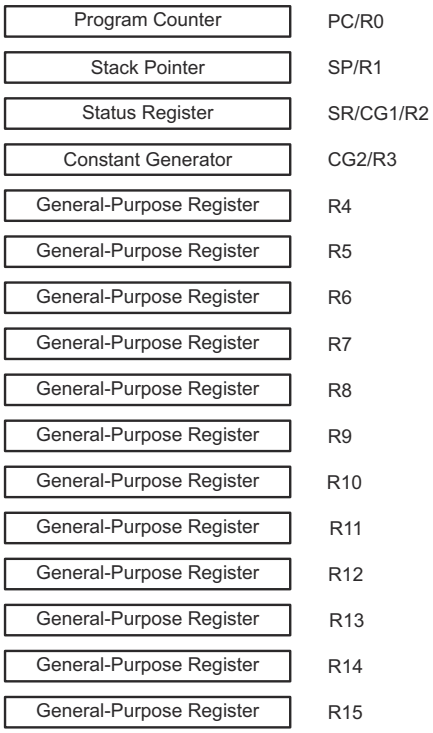


Figure 9-1. Integrated CPU Registers

9.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 9-1 lists examples of the three types of instruction formats, and Table 9-2 lists the address modes.

Table 9-1. Instruction Word Formats

INSTRUCTION WORD FORMAT	EXAMPLE	OPERATION
Dual operands, source and destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 9-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect auto-increment	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

9.4 Operating Modes

The devices have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No data retention
  - RTC enabled and clocked by low-frequency oscillator
  - Wake-up input from $\overline{\text{RST}}$/NMI, RTC_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, P1, P2, P3, and P4

9.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 9-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 9-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-up, External reset Watchdog time-out, key violation Flash memory key violation	WDTIFG, KEYV (SYSRSTIV)(1) (3)	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) (1) (3)	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV)(1) (2)	Maskable	0FFF8h	60
Timer TB0	TB0CCR0 CCIFG0(2)	Maskable	0FFF6h	59
Timer TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TBIV)(1) (2)	Maskable	0FFF4h	58
Watchdog interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (2)	Maskable	0FFF0h	56
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (2)	Maskable	0FFEEh	55
CTSD16	CTSD16IFG0, CTSD16OVIFG0(1) (2)	Maskable	0FFECh	54
Timer TA0	TA0CCR0 CCIFG0(2)	Maskable	0FFEAh	53
Timer TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (2)	Maskable	0FFE8h	52
USB_UBM(5)	USB interrupts (USBIV)(1) (2)	Maskable	0FFE6h	51
LDO-PWR (6)	LDOOFFIG, LDOONIFG, LDOOVLIFG			
DMA	DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG, DMA4IFG, DMA5IFG (DMAIV)(1) (2)	Maskable	0FFE4h	50
Timer TA1	TA1CCR0 CCIFG0(2)	Maskable	0FFE2h	49
Timer TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (2)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1) (2)	Maskable	0FFDEh	47
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (2)	Maskable	0FFDCh	46
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (2)	Maskable	0FFDAh	45
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)(1) (2)	Maskable	0FFD8h	44
LCD_B	LCD_B Interrupt Flags (LCDBIV)(1)	Maskable	0FFD6h	43
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1) (2)	Maskable	0FFD4h	42
DAC12_A	DAC12_0IFG, DAC12_1IFG(1) (2)	Maskable	0FFD2h	41
Timer TA2	TA2CCR0 CCIFG0(2)	Maskable	0FFD0h	40
Timer TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1) (2)	Maskable	0FFCEh	39
I/O port P3	P3IFG.0 to P3IFG.7 (P3IV)(1) (2)	Maskable	0FFCCh	38
I/O port P4	P4IFG.0 to P4IFG.7 (P4IV)(1) (2)	Maskable	0FFCAh	37
Reserved	Reserved(4)		0FFC8h	36
			⋮	⋮

Table 9-3. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
			0FF80h	0, lowest

(1) Multiple source flags
(2) Interrupt flags are in the module.
(3) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.
(5) Only on devices with peripheral module USB (MSP430FG6626 and MSP430FG6625)
(6) Only on devices with peripheral module LDO-PWR (MSP430FG6426 and MSP430FG6425)

9.6 USB BSL

The devices MSP430FG6626 and MSP430FG6625 are preprogrammed with the USB BSL. Use of the USB BSL requires external access to six pins (see Table 9-4). In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT, proper decoupling, and so on. For additional information, see the MSP430™ Flash Device Bootloader (BSL) User's Guide.

Table 9-4. USB BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
PU.0/DP	USB data terminal DP
PU.1/DM	USB data terminal DM
PUR	USB pullup resistor terminal
VBUS	USB bus power supply
VSSU	USB ground supply

Note

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-MΩ resistor to ground.

9.7 UART BSL

Devices without a USB module (MSP430FG642x) come preprogrammed with the UART BSL. A UART BSL is also available for devices with the USB module (MSP430FG662x), and it can be programmed by the user into the BSL memory by replacing the preprogrammed factory-supplied USB BSL. Use of the UART BSL requires external access to six pins (see Table 9-5). For additional information, see the MSP430™ Flash Device Bootloader (BSL) User's Guide.

Table 9-5. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

9.8 JTAG Operation

9.8.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 9-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide. For a complete description of the features of the JTAG interface and its implementation, see MSP430 Programming With the JTAG Interface.

Table 9-6. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

9.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 9-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide. For a complete description of the features of the JTAG interface and its implementation, see MSP430 Programming With the JTAG interface.

Table 9-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

9.9 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

9.10 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in Section 9.15.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

9.11 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the Battery Backup System module is implemented.

There are 8 bytes of backup RAM. It can be word-wise accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

9.12 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the MSP430F5xx and MSP430F6xx Family User's Guide.

9.12.1 Digital I/O

Up to nine 8-bit I/O ports are implemented: P1 through P9 are complete except P5.2, and port PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise (P1 through P8) in pairs (PA through PD).

9.12.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2 (see Table 9-8).

Table 9-8. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT	–	Comparator_B output
	PM_TB0CLK	Timer TB0 clock input	–
2	Reserved	–	Reserved
	PM_DMAE0	DMAE0 Input	–
3	PM_SVMOUT	–	SVM output
	PM_TB0OUTH	Timer TB0 high impedance input TB0OUTH	–
4	PM_TB0CCR0B	Timer TB0 CCR0 capture input CCI0B	Timer TB0: TB0.0 compare output Out0
5	PM_TB0CCR1B	Timer TB0 CCR1 capture input CCI1B	Timer TB0: TB0.1 compare output Out1
6	PM_TB0CCR2B	Timer TB0 CCR2 capture input CCI2B	Timer TB0: TB0.2 compare output Out2
7	PM_TB0CCR3B	Timer TB0 CCR3 capture input CCI3B	Timer TB0: TB0.3 compare output Out3
8	PM_TB0CCR4B	Timer TB0 CCR4 capture input CCI4B	Timer TB0: TB0.4 compare output Out4
9	PM_TB0CCR5B	Timer TB0 CCR5 capture input CCI5B	Timer TB0: TB0.5 compare output Out5
10	PM_TB0CCR6B	Timer TB0 CCR6 capture input CCI6B	Timer TB0: TB0.6 compare output Out6
11	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI – input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI – output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI – input)	
14	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I^2C clock (open drain and direction controlled by USCI)	
15	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I^2C data (open drain and direction controlled by USCI)	
16	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI – input)	
17	PM_MCLK	–	MCLK
18-30	Reserved	None	DVSS
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

Table 9-9 lists the default settings for all pins that support port mapping.

Table 9-9. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/P2MAP0	PM_UCB0STE, PM_UCA0CLK	USCI_B0 SPI slave transmit enable (direction controlled by USCI – input), USCI_A0 clock input/output (direction controlled by USCI)	
P2.1/P2MAP1	PM_UCB0SIMO, PM_UCB0SDA	USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 I^2C data (open drain and direction controlled by USCI)	
P2.2/P2MAP2	PM_UCB0SOMI, PM_UCB0SCL	USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 I^2C clock (open drain and direction controlled by USCI)	
P2.3/P2MAP3	PM_UCB0CLK, PM_UCA0STE	USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI – input)	
P2.4/P2MAP4	PM_UCA0TXD, PM_UCA0SIMO	USCI_A0 UART TXD (direction controlled by USCI – output), USCI_A0 SPI slave in master out (direction controlled by USCI)	
P2.5/P2MAP5/R23	PM_UCA0RXD, PM_UCA0SOMI	USCI_A0 UART RXD (direction controlled by USCI – input), USCI_A0 SPI slave out master in (direction controlled by USCI)	
P2.6/P2MAP6/R03	PM_NONE	-	DVSS
P2.7/P2MAP7/LCDREF/R13	PM_NONE	-	DVSS

9.12.3 Oscillator and System Clock

The clock system in the MSP430FG662x and MSP430FG642x devices are supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

9.12.4 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detect if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and the core supply.

9.12.5 Hardware Multiplier (MPY32)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

9.12.6 Real-Time Clock (RTC_B)

The RTC_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

9.12.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

9.12.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. Table 9-10 lists the SYS module interrupt vector registers.

Table 9-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	$\overline{\text{RST}}$/NMI (BOR)		04h	
	PMMSWBOR (BOR)		06h	
	LPM3.5 or LPM4.5 wake up (BOR)		08h	
	Security violation (BOR)		0Ah	
	SVSL (POR)		0Ch	
	SVSH (POR)		0Eh	
	SVML_OVP (POR)		10h	
	SVMH_OVP (POR)		12h	
	PMMSWPOR (POR)		14h	
	WDT time-out (PUC)		16h	
	WDT key violation (PUC)		18h	
	KEYV flash key violation (PUC)		1Ah	
	Reserved		1Ch	
	Peripheral area fetch (PUC)		1Eh	
	PMM key violation (PUC)		20h	
	Reserved		22h to 3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMLIFG		02h	Highest
	SVMHIFG		04h	
	DLYLIFG		06h	
	DLYHIFG		08h	
	VMAIFG		0Ah	
	JMBINIFG		0Ch	
	JMBOUTIFG		0Eh	
	SVMLVLRIFG		10h	

Table 9-10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
	SVMHVLRIFG		12h	
	Reserved		14h to 1Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	ACCVIFG		06h	
	BUSIFG		08h	
	Reserved		0Ah to 1Eh	Lowest
SYSBERRIV, Bus Error	No interrupt pending	0198h	00h	
	USB wait state time-out		02h	Highest
	Reserved		04h to 1Eh	Lowest

9.12.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also uses the channel 0, 1, and 2 DMA trigger assignments (see Table 9-11). The USB timestamp generator is available only on devices with the USB module (MSP430FG662x).

Table 9-11. DMA Trigger Assignments

TRIGGER(1)	CHANNEL					
	0	1	2	3	4	5
0	DMAREQ					
1	TA0CCR0 CCIFG					
2	TA0CCR2 CCIFG					
3	TA1CCR0 CCIFG					
4	TA1CCR2 CCIFG					
5	TA2CCR0 CCIFG					
6	TA2CCR2 CCIFG					
7	TBCCR0 CCIFG					
8	TBCCR2 CCIFG					
9	Reserved					
10	Reserved					
11	Reserved					
12	Reserved					
13	Reserved					
14	Reserved					
15	Reserved					
16	UCA0RXIFG					
17	UCA0TXIFG					
18	UCB0RXIFG					
19	UCB0TXIFG					
20	UCA1RXIFG					
21	UCA1TXIFG					
22	UCB1RXIFG					
23	UCB1TXIFG					
24	CTSD16IFG0					
25	DAC12_0IFG					
26	DAC12_1IFG					
27	USB FNRXD(2)					
28	USB ready(2)					
29	MPY ready					
30	DMA5IFG	DMA0IFG	DMA1IFG	DMA2IFG	DMA3IFG	DMA4IFG
31	DMAE0					

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

(2) Only on devices with peripheral module USB (MSP430FG662x), otherwise reserved (MSP430FG642x).

9.12.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I^2C.

The MSP430FG662x and MSP430FG642x include two complete USCI modules (n = 0 to 1).

9.12.11 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 supports multiple capture/compares, PWM outputs, and interval timing (see Table 9-12). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-12. Timer TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZCA, ZQW						PZ	ZCA, ZQW
34-P1.0	L5-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
34-P1.0	L5-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
35-P1.1	M5-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	35-P1.1	M5-P1.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
36-P1.2	J6-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	36-P1.2	J6-P1.2
40-P1.6	J7-P1.6	TA0.1	CCI1B				40-P1.6	J7-P1.6
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
37-P1.3	H6-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	37-P1.3	H6-P1.3
41-P1.7	M7-P1.7	TA0.2	CCI2B				41-P1.7	M7-P1.7
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
38-P1.4	M6-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	38-P1.4	M6-P1.4
		DV_{SS}	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
39-P1.5	L6-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	39-P1.5	L6-P1.5
		DV_{SS}	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

9.12.12 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 supports multiple capture/compares, PWM outputs, and interval timing (see Table 9-13). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-13. Timer TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZCA, ZQW						PZ	ZCA, ZQW
42-P3.0	L7-P3.0	TA1CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
42-P3.0	L7-P3.0	TA1CLK	$\overline{\text{TACLK}}$					
43-P3.1	H7-P3.1	TA1.0	CCI0A	CCR0	TA0	TA1.0	43-P3.1	H7-P3.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
44-P3.2	M8-P3.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	44-P3.2	M8-P3.2
		CBOUT (internal)	CCI1B				DAC12_A DAC12_0, DAC12_1 (internal)	
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
45-P3.3	L8-P3.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	45-P3.3	L8-P3.3
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

9.12.13 Timer TA2

Timer TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 supports multiple capture/compares, PWM outputs, and interval timing (see Table 9-14). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-14. Timer TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZCA, ZQW						PZ	ZCA, ZQW
46-P3.4	J8-P3.4	TA2CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
46-P3.4	J8-P3.4	TA2CLK	$\overline{\text{TACLK}}$					
47-P3.5	M9-P3.5	TA2.0	CCI0A	CCR0	TA0	TA2.0	47-P3.5	M9-P3.5
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
48-P3.6	L9-P3.6	TA2.1	CCI1A	CCR1	TA1	TA2.1	48-P3.6	L9-P3.6
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
49-P3.7	M10-P3.7	TA2.2	CCI2A	CCR2	TA2	TA2.2	49-P3.7	M10-P3.7
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

9.12.14 Timer TB0

Timer TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 supports multiple capture/compares, PWM outputs, and interval timing (see Table 9-15). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-15. Timer TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZCA, ZQW						PZ	ZCA, ZQW
58-P8.0 P2MAPx(1)	J11-P8.0 P2MAPx(1)	TB0CLK	TB0CLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
58-P8.0 P2MAPx(1)	J11-P8.0 P2MAPx(1)	TB0CLK	$\overline{\text{TB0CLK}}$					
50-P4.0	J9-P4.0	TB0.0	CCI0A	CCR0	TB0	TB0.0	50-P4.0	J9-P4.0
P2MAPx(1)	P2MAPx(1)	TB0.0	CCI0B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
51-P4.1	M11-P4.1	TB0.1	CCI1A	CCR1	TB1	TB0.1	51-P4.1	M11-P4.1
P2MAPx(1)	P2MAPx(1)	TB0.1	CCI1B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
52-P4.2	L10-P4.2	TB0.2	CCI2A	CCR2	TB2	TB0.2	52-P4.2	L10-P4.2
P2MAPx(1)	P2MAPx(1)	TB0.2	CCI2B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND				DAC12_A DAC12_0, DAC12_1 (internal)	
		DV_{CC}	V_{CC}					
53-P4.3	M12-P4.3	TB0.3	CCI3A	CCR3	TB3	TB0.3	53-P4.3	M12-P4.3
P2MAPx(1)	P2MAPx(1)	TB0.3	CCI3B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
54-P4.4	L12-P4.4	TB0.4	CCI4A	CCR4	TB4	TB0.4	54-P4.4	L12-P4.4
P2MAPx(1)	P2MAPx(1)	TB0.4	CCI4B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
55-P4.5	L11-P4.5	TB0.5	CCI5A	CCR5	TB5	TB0.5	55-P4.5	L11-P4.5
P2MAPx(1)	P2MAPx(1)	TB0.5	CCI5B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
56-P4.6	K11-P4.6	TB0.6	CCI6A	CCR6	TB6	TB0.6	56-P4.6	K11-P4.6
P2MAPx(1)	P2MAPx(1)	TB0.6	CCI6B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

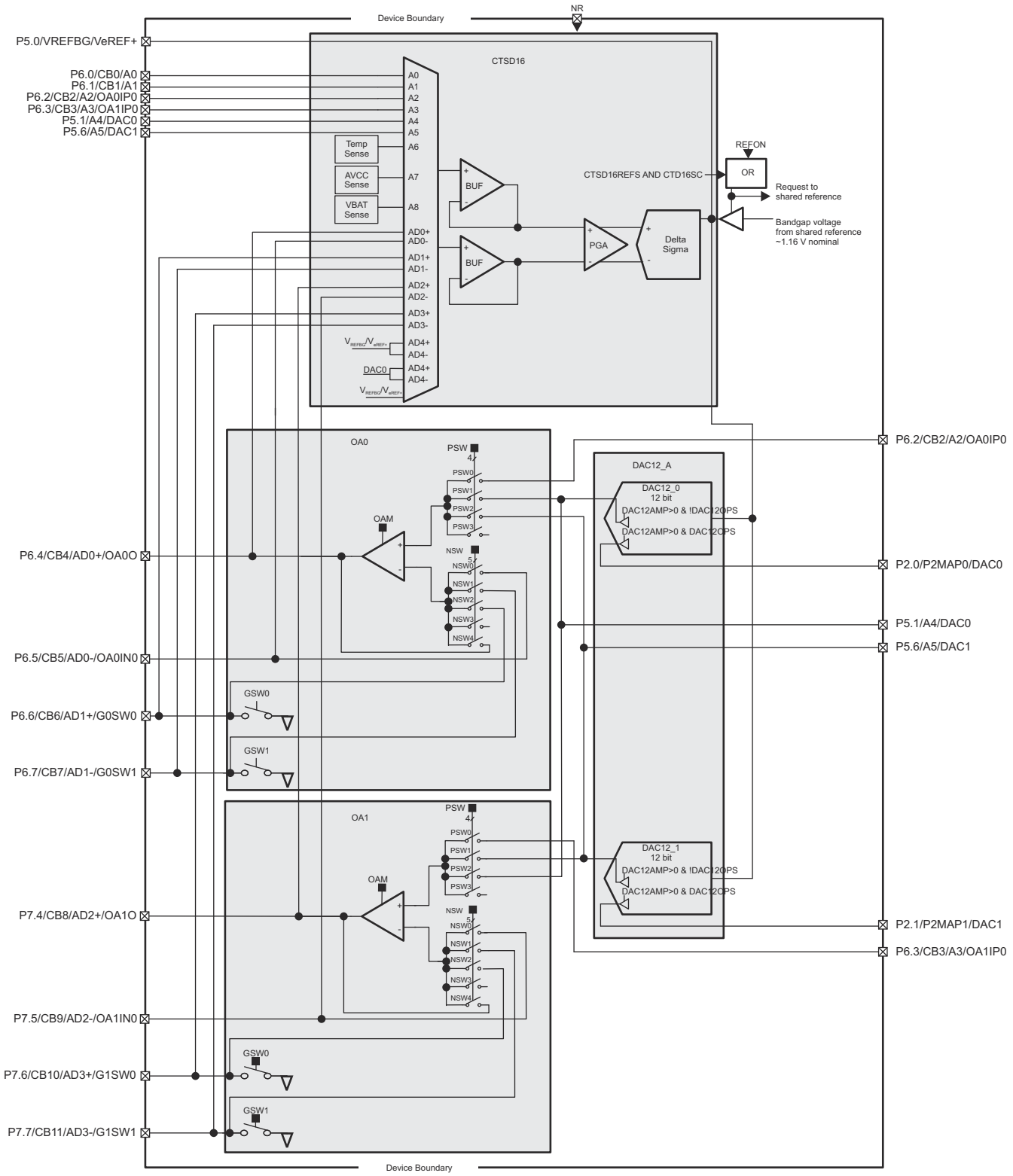
(1) Timer functions are selectable by the port mapping controller.

9.12.15 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

9.12.16 Signal Chain

All devices include all the building blocks to construct a complete signal chain. These blocks include two digital-to-analog converter (DAC) channels, two integrated operational amplifiers (OAs), a sigma-delta analog-to-digital converter (CTSD16), and low-ohmic switches (GSW). Figure 9-2 shows the various signal chain blocks and their interconnections in the overall system.



A. See the MSP430F5xx and MSP430F6xx Family User's Guide for additional module details.

Figure 9-2. Signal Chain

9.12.16.1 CTSD16

The CTSD16 module integrates a single sigma-delta ADC with ten external inputs and four internal inputs. The converter is designed with a fully differential analog input pair and a programmable gain amplifier input stage. The converter is based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 256.

The CTSD16 is proceeded by an analog multiplexer which is used for channel selection, followed by a unity gain buffer stage useful when sampling high impedance sensors.

The CTSD16 can use as its reference the internal bandgap voltage from the REF module or an external reference at the VeREF+ pin.

9.12.16.2 DAC12_A

The DAC12_A module is a 12-bit R-ladder voltage-output DAC. The DAC12_A can be used in 8-bit or 12-bit mode, and can be used in conjunction with the DMA controller. When multiple DAC12_A modules are present, they may be grouped together for synchronous operation. Two complete channels are available, DAC12_0 and DAC12_1.

9.12.16.3 Operational Amplifiers (OA)

The device integrates two low-power operational amplifiers. The operational amplifiers can perform signal conditioning of low-level analog signals before conversion by the ADC. Each operational amplifier can be individually controlled by software.

9.12.16.4 Ground Switches (GSW)

The device integrates four low-ohmic switches to ground that are individually controllable in software. These can switch in and out various components in the measurement system.

9.12.17 REF Voltage Reference

The reference module (REF) generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

9.12.18 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

9.12.19 LCD_B

The LCD_B driver generates the segment and common signals that are required to drive a liquid crystal display (LCD). The LCD_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments.

9.12.20 USB Universal Serial Bus

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

The USB module is only available on the MSP430FG662x devices.

9.12.21 LDO and PU Port

The integrated 3.3-V power system incorporates an integrated 3.3-V LDO regulator that allows the entire MSP430 microcontroller to be powered from nominal 5-V LDOI when it is made available for the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether.

The Port U pins (PU.0 and PU.1) function as general-purpose high-current I/O pins. These pins must be configured together as either both inputs or both outputs. Port U is supplied by the LDOO rail. If the 3.3-V LDO is not used in the system (disabled), the LDOO pin can be supplied externally.

The LDO-PWR module (LDO and PU port) is available only on the MSP430FG6426 and MSP430FG6425 devices.

9.12.22 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access.
- Two hardware triggers or breakpoints on CPU register write access.
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints.
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

9.13 Input/Output Diagrams

9.13.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 9-3 shows the port diagram. Table 9-16 summarizes the selection of the port function.

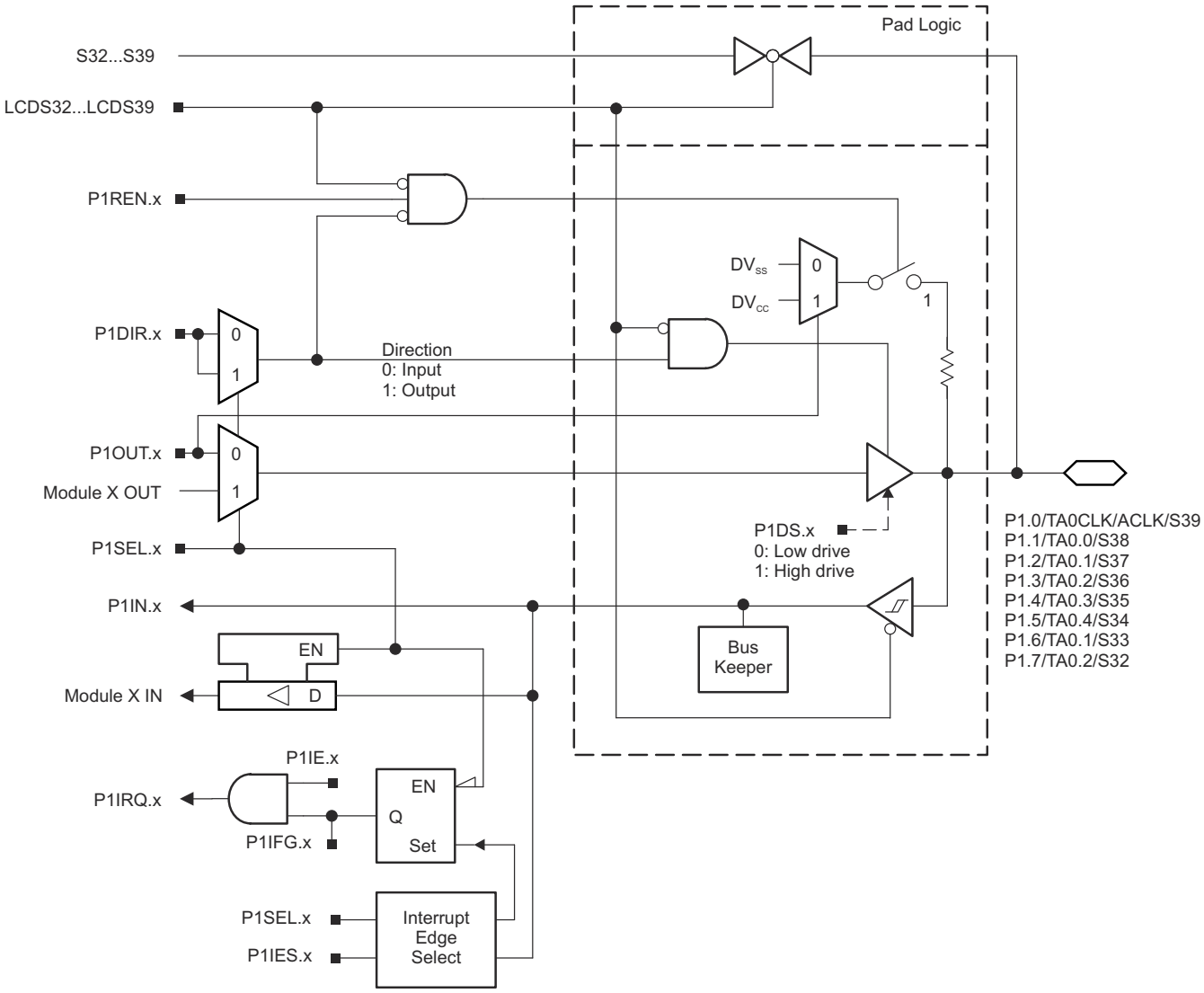


Figure 9-3. Port P1 (P1.0 to P1.7) Diagram

Table 9-16. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	LCDS32 to LCDS39
P1.0/TA0CLK/ACLK/S39	0	P1.0 (I/O)	I: 0; O: 1	0	0
		Timer TA0.TA0CLK	0	1	0
		ACLK	1	1	0
		S39	X	X	1
P1.1/TA0.0/S38	1	P1.1 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI0A capture input	0	1	0
		Timer TA0.0 output	1	1	0
		S38	X	X	1
P1.2/TA0.1/S37	2	P1.2 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI1A capture input	0	1	0
		Timer TA0.1 output	1	1	0
		S37	X	X	1
P1.3/TA0.2/S36	3	P1.3 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI2A capture input	0	1	0
		Timer TA0.2 output	1	1	0
		S36	X	X	1
P1.4/TA0.3/S35	4	P1.4 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI3A capture input	0	1	0
		Timer TA0.3 output	1	1	0
		S35	X	X	1
P1.5/TA0.4/S34	5	P1.5 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI4A capture input	0	1	0
		Timer TA0.4 output	1	1	0
		S34	X	X	1
P1.6/TA0.1/S33	6	P1.6 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI1B capture input	0	1	0
		Timer TA0.1 output	1	1	0
		S33	X	X	1
P1.7/TA0.2/S32	7	P1.7 (I/O)	I: 0; O: 1	0	0
		Timer TA0.CCI2B capture input	0	1	0
		Timer TA0.2 output	1	1	0
		S32	X	X	1

(1) X= don't care

9.13.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 9-4 shows the port diagram. Table 9-17 summarizes the selection of the port function.

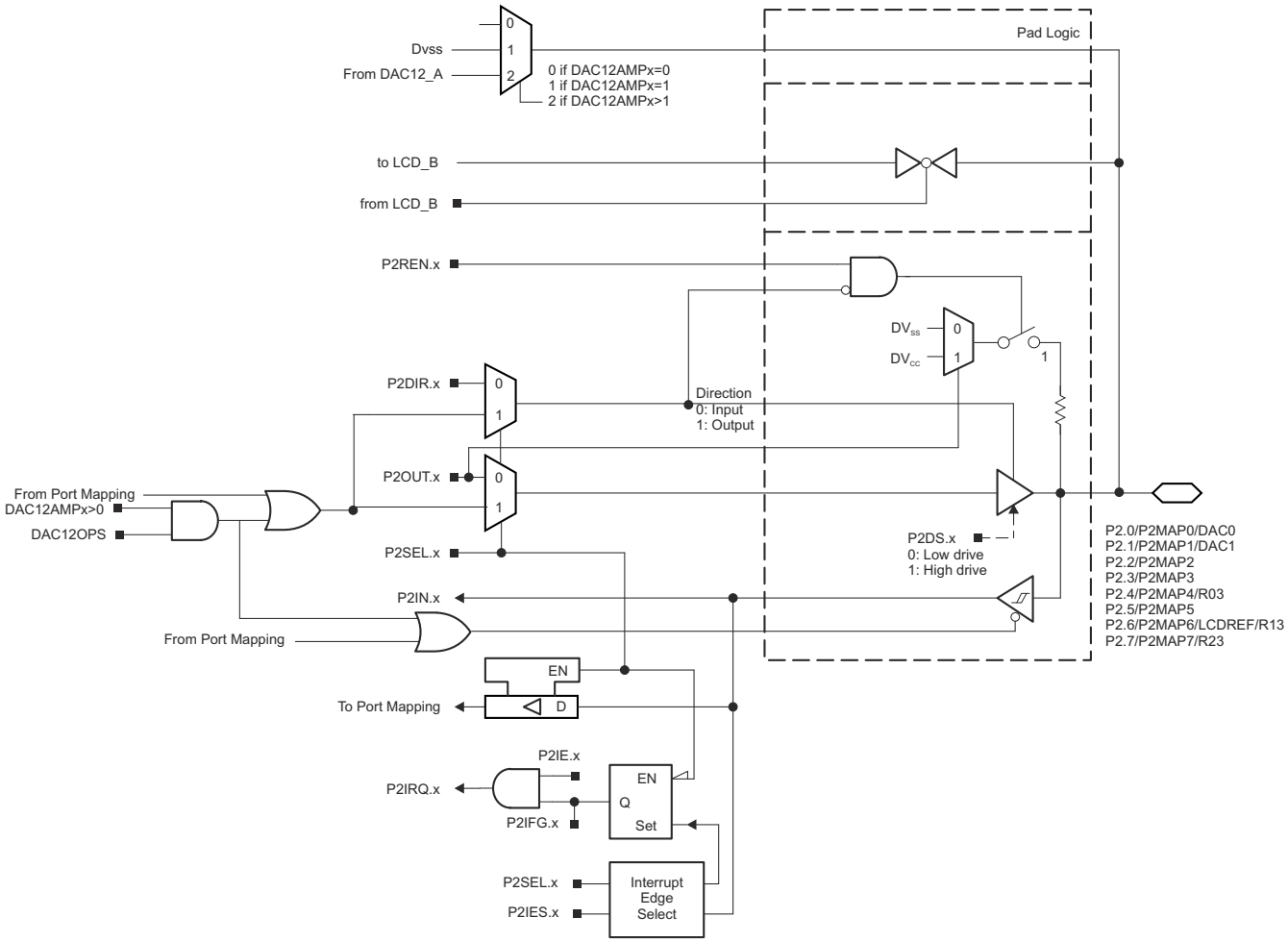


Figure 9-4. Port P2 (P2.0 to P2.7) Diagram

Table 9-17. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]				
			P2DIR.x	P2SEL.x	P2MAPx	DAC12OPS	DAC12AMPx
P2.0/P2MAP0/DAC0	0	P2.0 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
		DAC0	X	X	= 31	1	>1
P2.1/P2MAP1/DAC1	1	P2.1 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
		DAC1	X	X	= 31	1	>1
P2.2/P2MAP2	2	P2.2 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
P2.3/P2MAP3	3	P2.3 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
P2.4/P2MAP4/R03	4	P2.4 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
		R03	X	1	= 31	X	0
P2.5/P2MAP5	5	P2.5 (I/O	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
P2.6/P2MAP6/LCDREF/R13	6	P2.6 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
		LCDREF/R13	X	1	= 31	X	0
P2.7/P2MAP7/R23	7	P2.7 (I/O)	I: 0; O: 1	0		X	0
		Mapped secondary digital function	X	1	≤ 19	X	0
		R23	X	1	= 31	X	0

(1) X= Don't care

9.13.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Figure 9-5 shows the port diagram. Table 9-18 summarizes the selection of the port function.

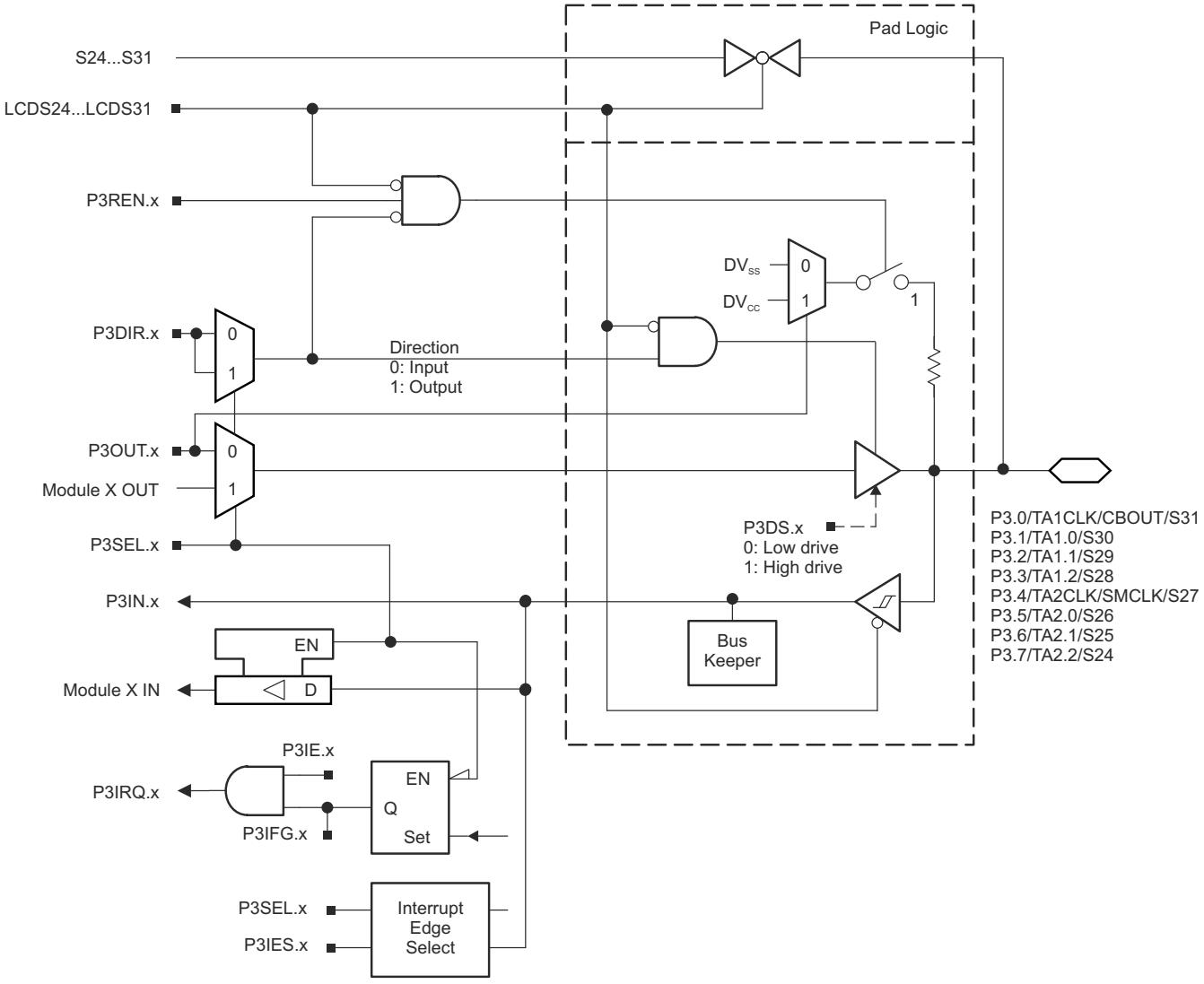


Figure 9-5. Port P3 (P3.0 to P3.7) Diagram

Table 9-18. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P3DIR.x	P3SEL.x	LCDS24 to LCDS31
P3.0/TA1CLK/CBOUT/S31	0	P3.0 (I/O)	I: 0; O: 1	0	0
		Timer TA1.TA1CLK	0	1	0
		CBOUT	1	1	0
		S31	X	X	1
P3.1/TA1.0/S30	1	P3.1 (I/O)	I: 0; O: 1	0	0
		Timer TA1.CCI0A capture input	0	1	0
		Timer TA1.0 output	1	1	0
		S30	X	X	1
P3.2/TA1.1/S29	2	P3.2 (I/O)	I: 0; O: 1	0	0
		Timer TA1.CCI1A capture input	0	1	0
		Timer TA1.1 output	1	1	0
		S29	X	X	1
P3.3/TA1.2/S28	3	P3.3 (I/O)	I: 0; O: 1	0	0
		Timer TA1.CCI2A capture input	0	1	0
		Timer TA1.2 output	1	1	0
		S28	X	X	1
P3.4/TA2CLK/SMCLK/S27	4	P3.4 (I/O)	I: 0; O: 1	0	0
		Timer TA2.TA2CLK	0	1	0
		SMCLK	1	1	0
		S27	X	X	1
P3.5/TA2.0/S26	5	P3.5 (I/O)	I: 0; O: 1	0	0
		Timer TA2.CCI0A capture input	0	1	0
		Timer TA2.0 output	1	1	0
		S26	X	X	1
P3.6/TA2.1/S25	6	P3.6 (I/O)	I: 0; O: 1	0	0
		Timer TA2.CCI1A capture input	0	1	0
		Timer TA2.1 output	1	1	1
		S25	X	X	1
P3.7/TA2.2/S24	7	P3.7 (I/O)	I: 0; O: 1	0	0
		Timer TA2.CCI2A capture input	0	1	0
		Timer TA2.2 output	1	1	0
		S24	X	X	1

(1) X= don't care

9.13.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 9-6 shows the port diagram. Table 9-19 summarizes the selection of the port function.

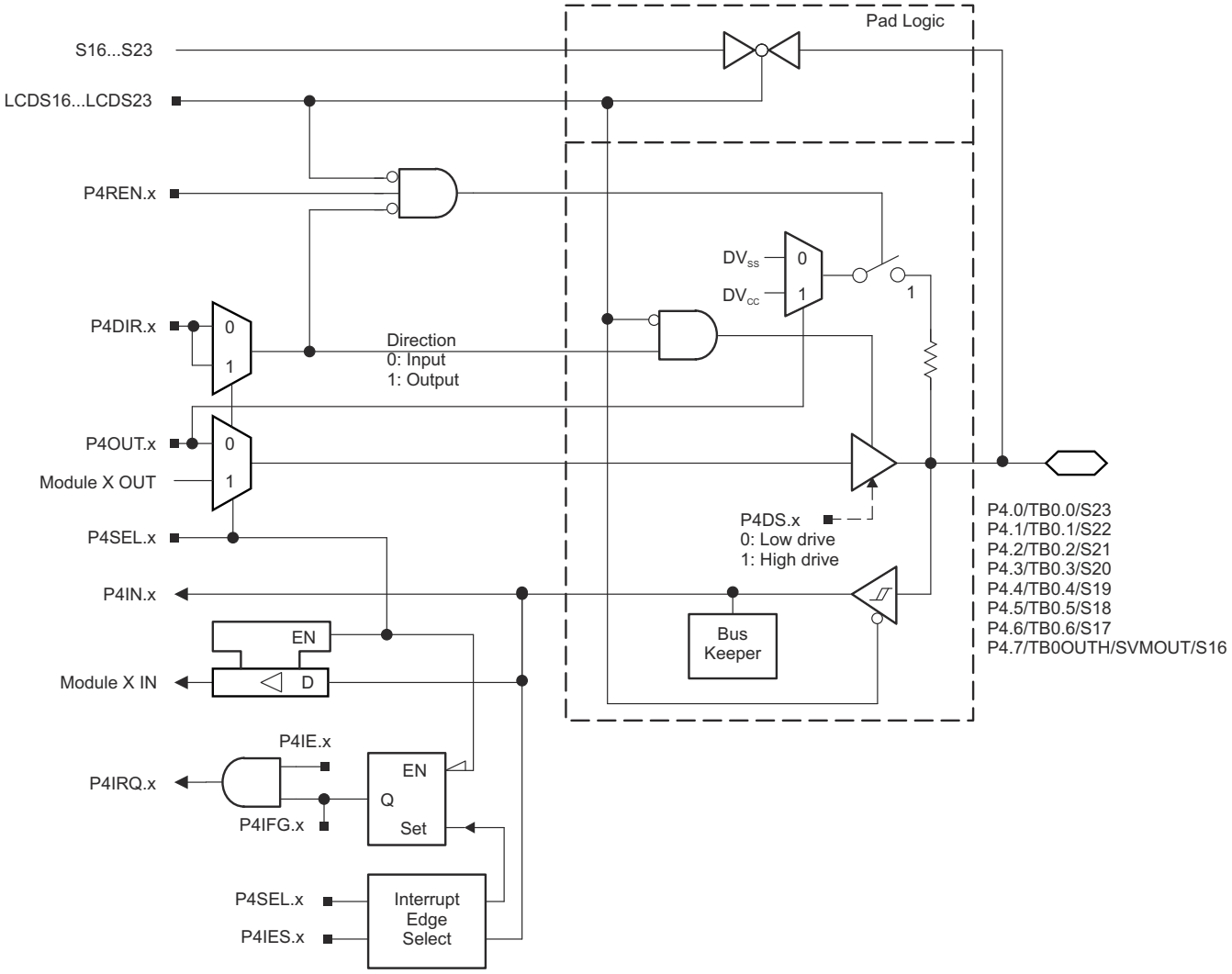


Figure 9-6. Port P4 (P4.0 to P4.7) Diagram

Table 9-19. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL.x	LCDS16 to LCDS23
P4.0/TB0.0/S23	0	P4.0 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI0A capture input	0	1	0
		Timer TB0.0 output(2)	1	1	0
		S23	X	X	1
P4.1/TB0.1/S22	1	P4.1 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI1A capture input	0	1	0
		Timer TB0.1 output(2)	1	1	0
		S22	X	X	1
P4.2/TB0.2/S21	2	P4.2 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI2A capture input	0	1	0
		Timer TB0.2 output(2)	1	1	0
		S21	X	X	1
P4.3/TB0.3/S20	3	P4.3 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI3A capture input	0	1	0
		Timer TB0.3 output(2)	1	1	0
		S20	X	X	1
P4.4/TB0.4/S19	4	P4.4 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI4A capture input	0	1	0
		Timer TB0.4 output(2)	1	1	0
		S19	X	X	1
P4.5/TB0.5/S18	5	P4.5 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI5A capture input	0	1	0
		Timer TB0.5 output(2)	1	1	0
		S18	X	X	1
P4.6/TB0.6/S17	6	P4.6 (I/O)	I: 0; O: 1	0	0
		Timer TB0.CCI6A capture input	0	1	0
		Timer TB0.6 output(2)	1	1	0
		S17	X	X	1
P4.7/TB0OUTH/ SVMOUT/S16	7	P4.7 (I/O)	I: 0; O: 1	0	0
		Timer TB0.TB0OUTH	0	1	0
		SVMOUT	1	1	0
		S16	X	X	1

(1) X= don't care
(2) Setting TB0OUTH causes all Timer_B configured outputs to be set to high impedance.

9.13.5 Port P5 (P5.0) Input/Output With Schmitt Trigger

Figure 9-7 shows the port diagram. Table 9-20 summarizes the selection of the port function.

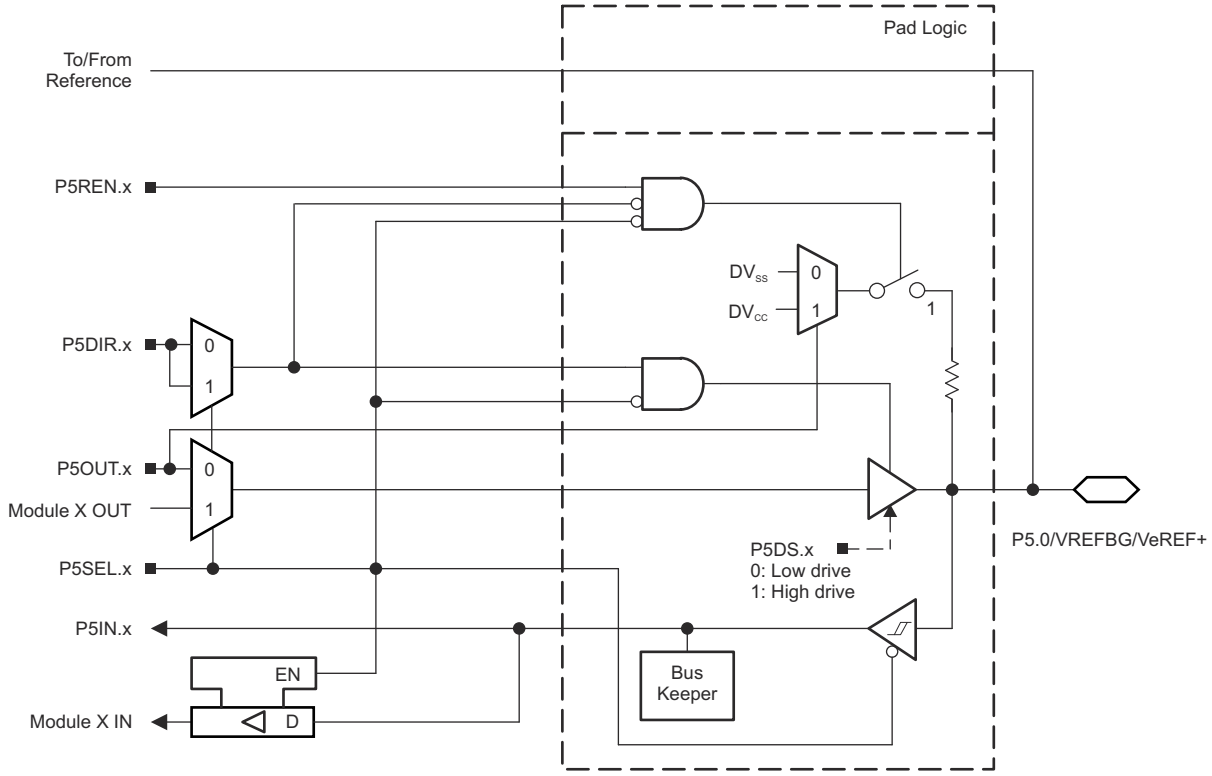


Figure 9-7. Port P5 (P5.0) Diagram

Table 9-20. Port P5 (P5.0) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				
			P5DIR.x	P5SEL.x	REFOUT	REFON(5)	CTSD16REFS(6)
P5.0/VREFBG/VeREF+	0	P5.0 (I/O)(2)	I: 0; O: 1	0	X	X	X
		VeREF+(3)	X	1	0	X	0
		VREFBG(4)	X	1	1	1	1

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the CTSD16 or DAC.
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The internal reference voltage signal, V_{REFBG}, is available at the pin.
(5) If a module is requesting a reference then REFON need not be set to 1 for VREFBG to be selected on P5.0.
(6) If CTSD16 is active, this bit must be set as shown in the table. Otherwise if set to 1, it will force VREFBG to be selected regardless of REFOUT setting and if P5SEL.x is set to 0 it will cause possible contention on the I/O.

9.13.6 Port P5 (P5.1 and P5.6) Input/Output With Schmitt Trigger

Figure 9-8 shows the port diagram. Table 9-21 summarizes the selection of the port function.

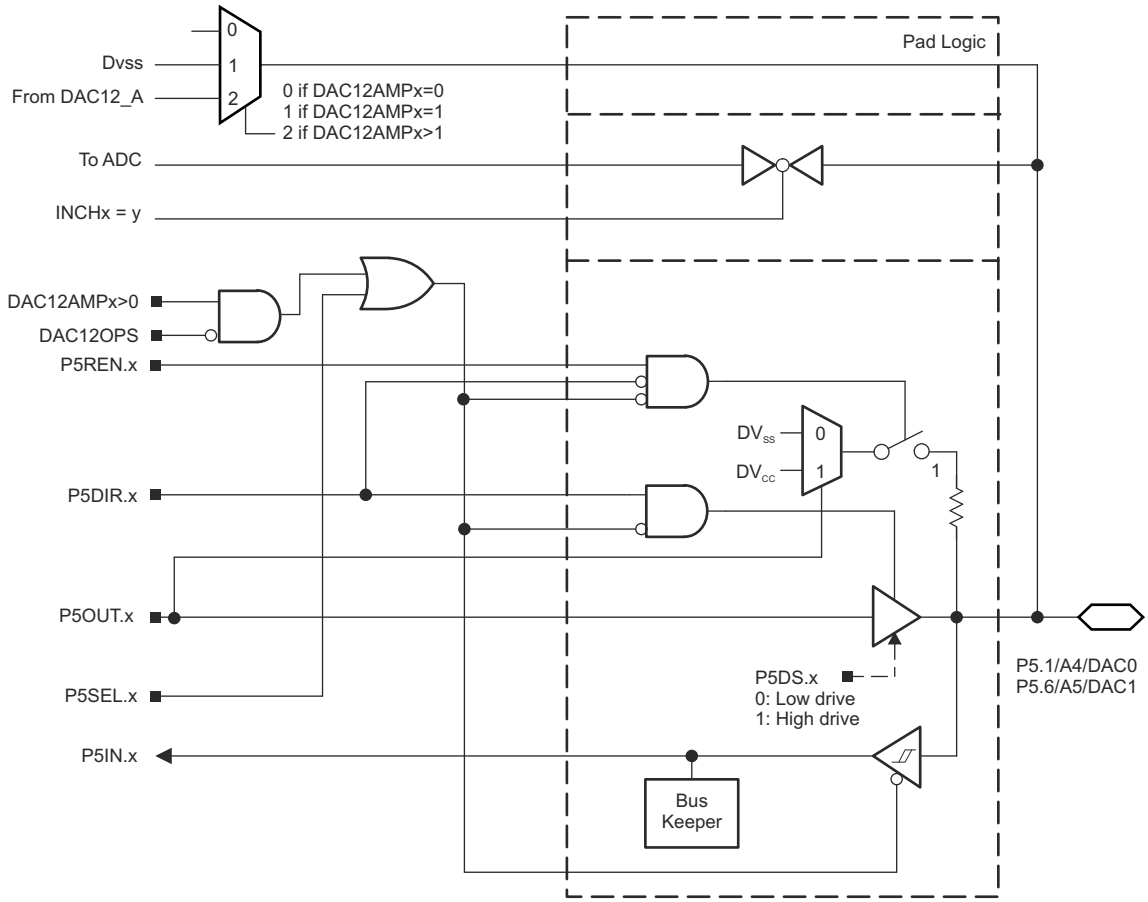


Figure 9-8. Port P5 (P5.1 and P5.6) Diagram

Table 9-21. Port P5 (P5.1 and P5.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P5DIR.x	P5SEL.x	DAC12OPS	DAC12AMPx
P5.1/A4/DAC0	1	P5.1(I/O)	I: 0; O: 1	0	X	0
		A4(2) (3)	X	1	X	0
		DAC0	X	X	0	>1
P5.6/A5/DAC1	1	P5.6(I/O)	I: 0; O: 1	0	X	0
		A5(2) (3)	X	1	X	0
		DAC1	X	X	0	>1

(1) X = Don't care
(2) Setting the P5SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

9.13.7 Port P5 (P5.3 to P5.5, P5.7) Input/Output With Schmitt Trigger

Figure 9-9 shows the port diagram. Table 9-22 summarizes the selection of the port function.

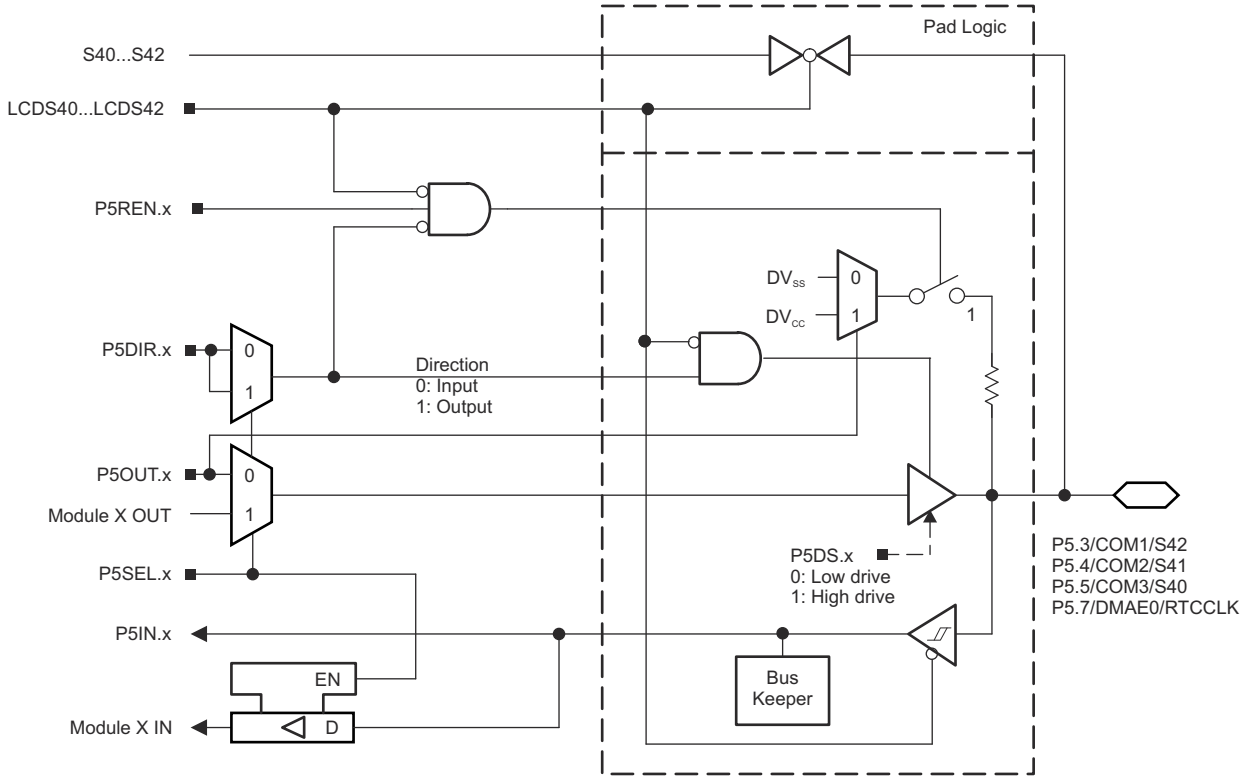


Figure 9-9. Port P5 (P5.3 to P5.5 and P5.7) Diagram

Table 9-22. Port P5 (P5.3 to P5.5, P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P5DIR.x	P5SEL.x	LCDS40 to LCDS42
P5.3/COM1/S42	3	P5.3 (I/O)	I: 0; O: 1	0	0
		COM1	X	1	X
		S42	X	0	1
P5.4/COM2/S41	4	P5.4 (I/O)	I: 0; O: 1	0	0
		COM2	X	1	X
		S41	X	0	1
P5.5/COM3/S40	5	P5.5 (I/O)	I: 0; O: 1	0	0
		COM3	X	1	X
		S40	X	0	1
P5.7/DMAE0/RTCCLK	7	P5.7 (I/O)	I: 0; O: 1	0	na
		DMAE0	0	1	na
		RTCCLK	1	1	na

9.13.8 Port P6 (P6.0 to P6.1) Input/Output With Schmitt Trigger

Figure 9-10 shows the port diagram. Table 9-23 summarizes the selection of the port function.

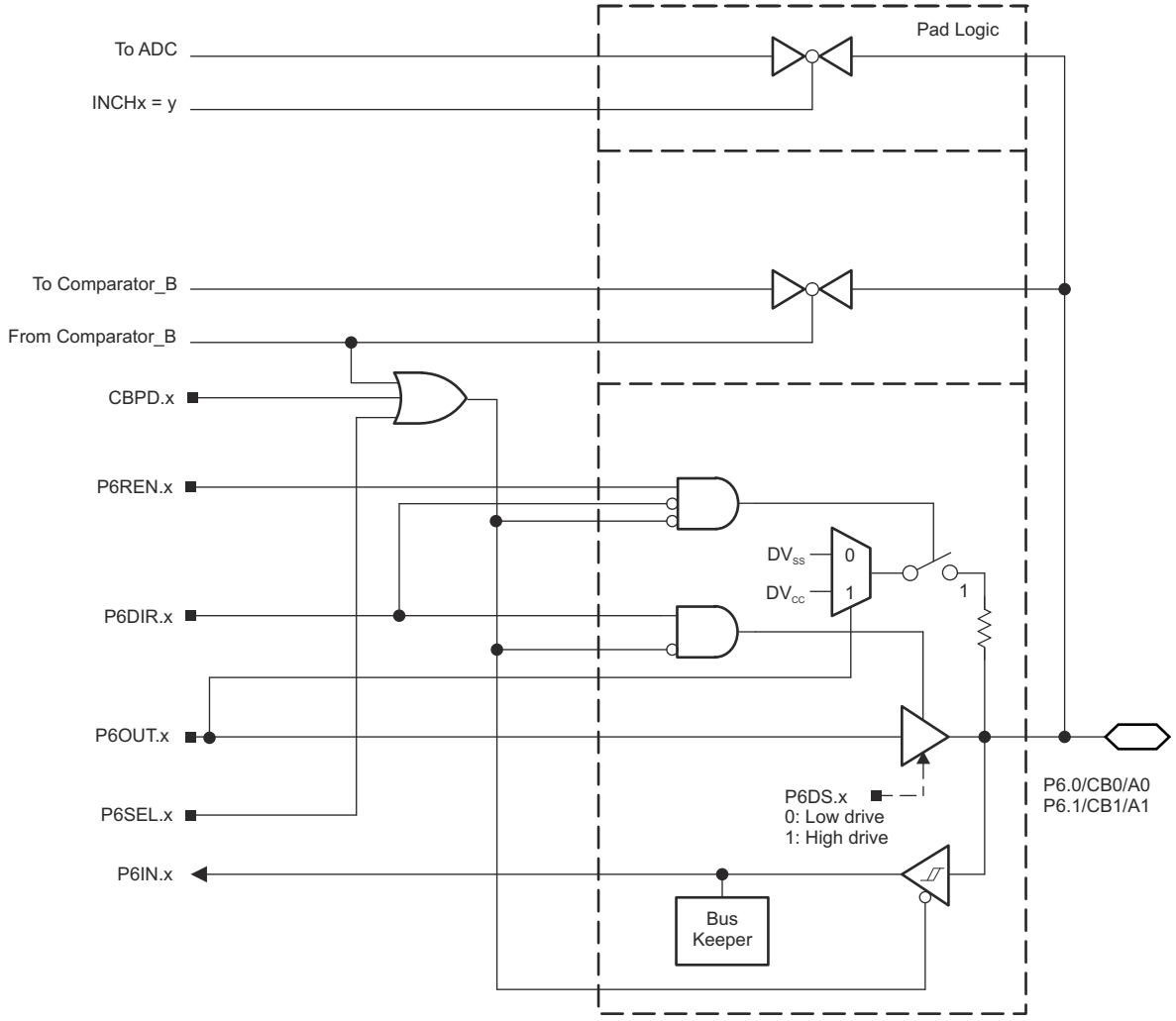


Figure 9-10. Port P6 (P6.0 to P6.1) Diagram

Table 9-23. Port P6 (P6.0 to P6.1) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL.x	CBPD.x
P6.0/CB0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	0
		CB0	X	X	1
		A0(2) (3)	X	1	X
P6.1/CB1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	0
		CB1	X	X	1
		A1(2) (3)	X	1	X

(1) X= Don't care
(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

9.13.9 Port P6 (P6.2 and P6.3) Input/Output With Schmitt Trigger

Figure 9-11 shows the port diagram. Table 9-24 summarizes the selection of the port function.

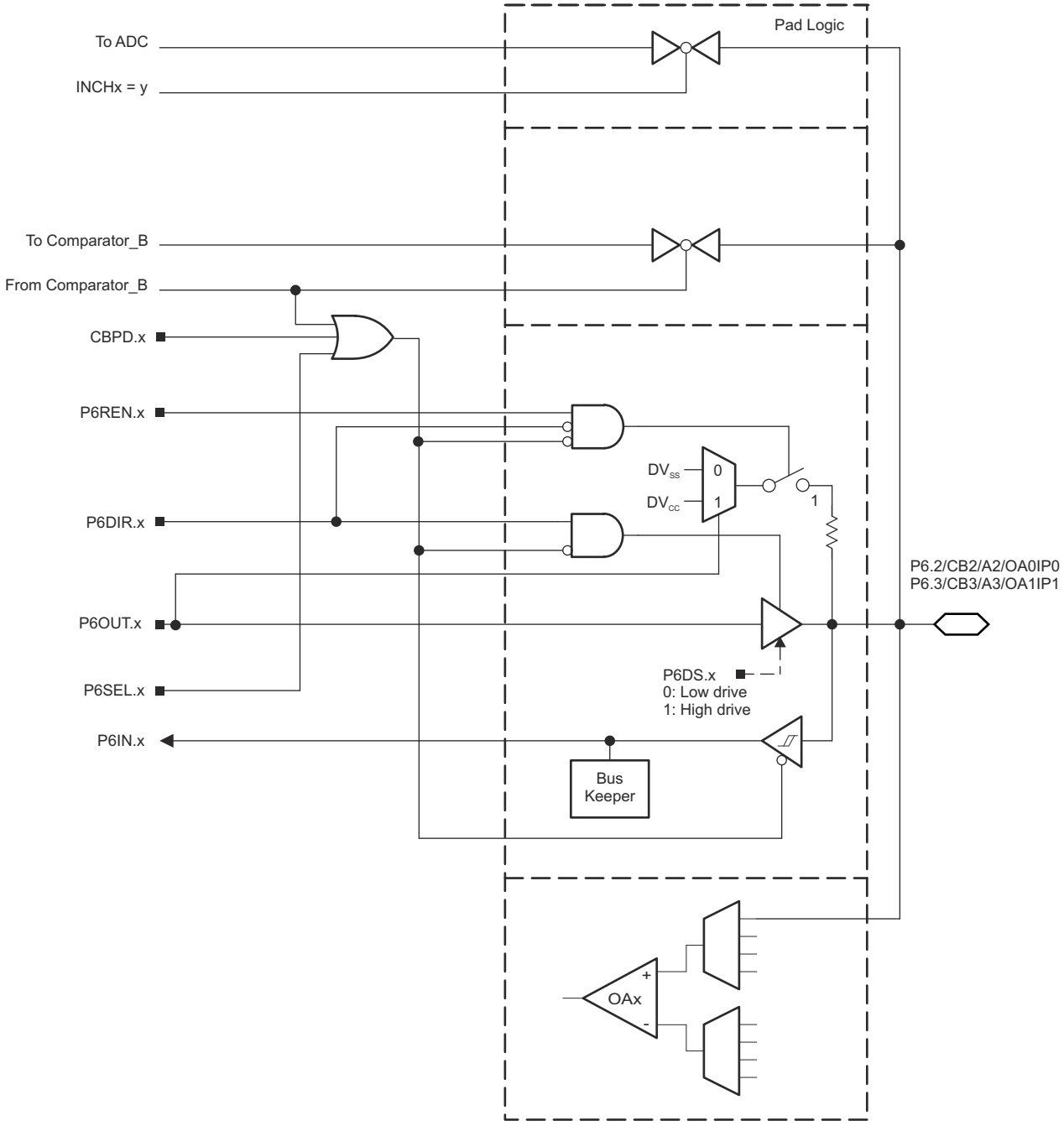


Figure 9-11. Port P6 (P6.2 and P6.3) Diagram

Table 9-24. Port P6 (P6.2 and P6.3) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL.x(3)	CBPD.x(3)
P6.2/CB2/A2/OA0IP0	2	P6.2 (I/O)	I: 0; O: 1	0	0
		CB2	X	X	1
		A2 (2)	X	1	X
		OA0IP0(3)	X	1	X
P6.3/CB3/A3/OA1IP0	3	P6.2 (I/O)	I: 0; O: 1	0	0
		CB3	X	X	1
		A3 (3)	X	1	X
		OA1IP0(3)	X	1	X

(1) X = Don't care
(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
(3) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

9.13.10 Port P6 (P6.4) Input/Output With Schmitt Trigger

Figure 9-12 shows the port diagram. Table 9-25 summarizes the selection of the port function.

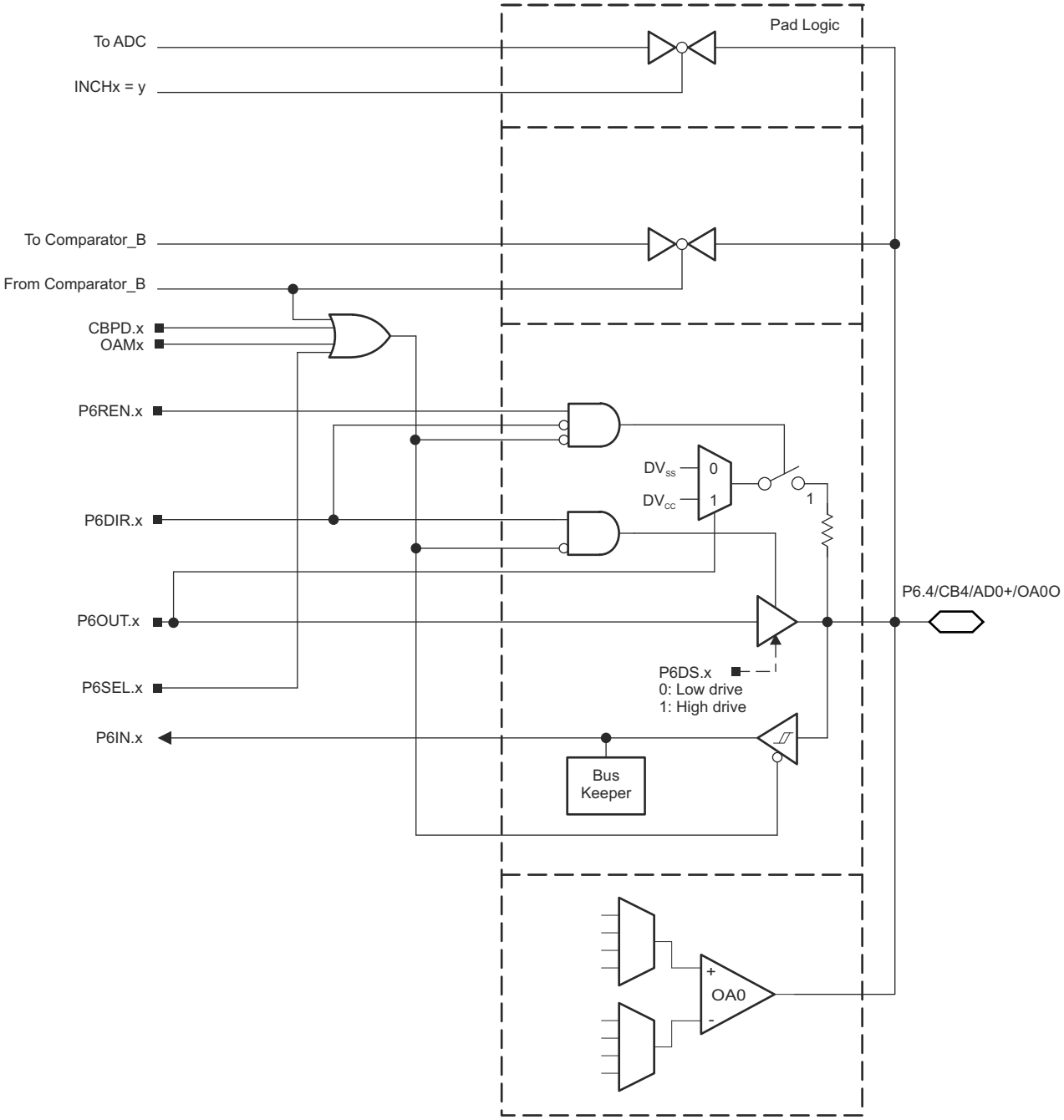


Figure 9-12. Port P6 (P6.4) Diagram

Table 9-25. Port P6 (P6.4) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P6DIR.x	P6SEL.x[3]	CBPD.x[3]	OAMx
P6.4/CB4/AD0+/OA0O	4	P6.4 (I/O)	I: 0; O: 1	0	0	0[4]
		CB4	X	X	1	0[4]
		AD0+ [2]	X	1	X	0[4]
		OA0O	X	X	X	= 1[4]

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting the P6SEL.x bit, the CBPD.x bit, or the OAMx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the output voltage of the amplifier.

9.13.11 Port P6 (P6.5) Input/Output With Schmitt Trigger

Figure 9-13 shows the port diagram. Table 9-26 summarizes the selection of the port function.

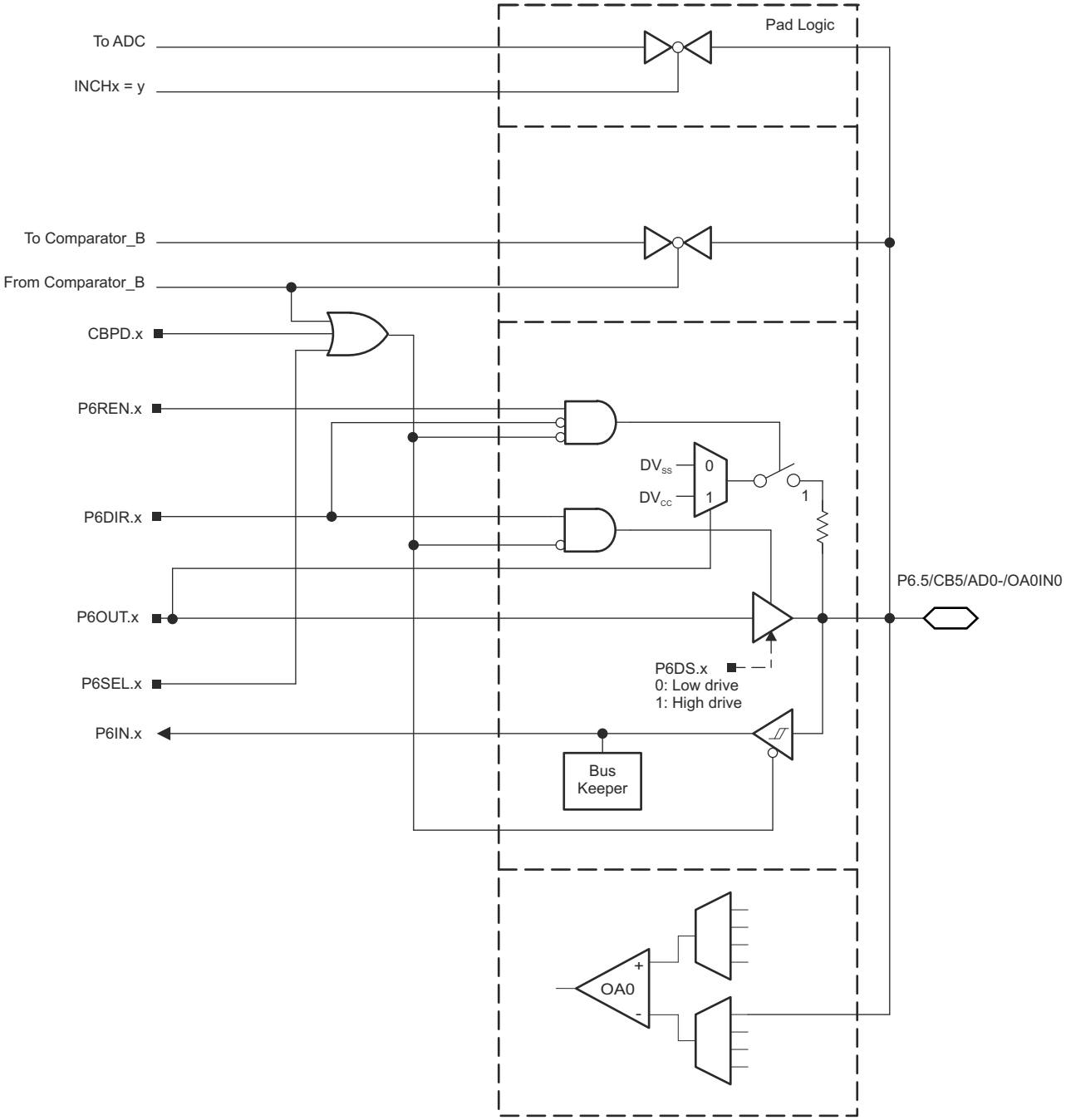


Figure 9-13. Port P6 (P6.5) Diagram

Table 9-26. Port P6 (P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL.x(3)	CBPD.x(3)
P6.5/CB5/AD0-/OA0IN0	5	P6.5 (I/O)	I: 0; O: 1	0	0
		CB5	X	X	1
		AD0- (2)	X	1	X
		OA0IN0(3)	X	1	X

(1) X = Don't care
(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
(3) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

9.13.12 Port P6 (P6.6) Input/Output With Schmitt Trigger

Figure 9-14 shows the port diagram. Table 9-27 summarizes the selection of the port function.

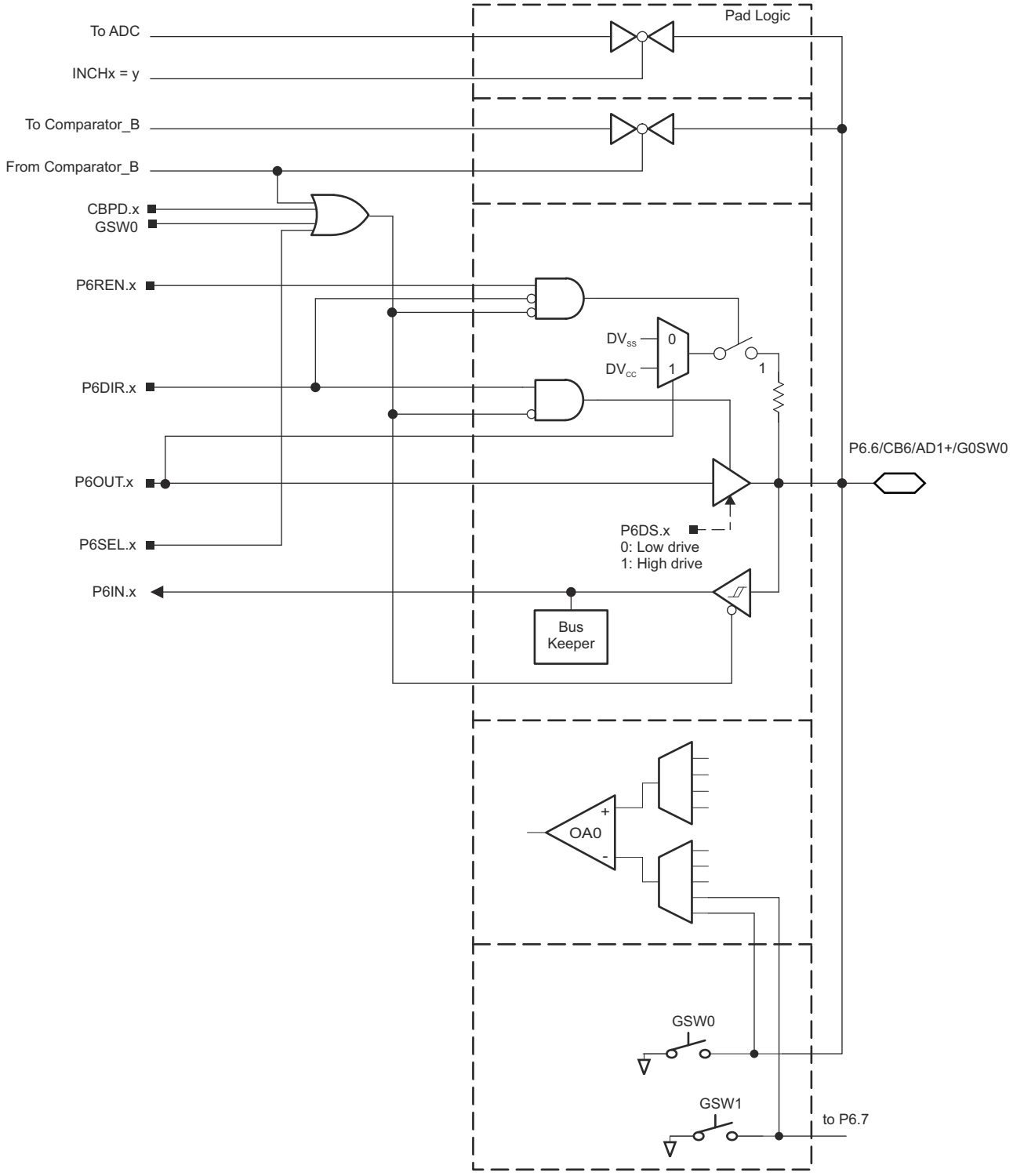


Figure 9-14. Port P6 (P6.6) Diagram

Table 9-27. Port P6 (P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P6SEL.x(3)	CBPD.x(3)	GSW0(3)
P6.6/CB6/AD1+/G0SW0	6	P6.6 (I/O)	I: 0; O: 1	0	0	0
		CB6	X	X	1	0
		AD1+ (2)	X	1	X	0
		G0SW0(4)	X	X	X	1

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting the P6SEL.x bit, the CBPD.x bit, or the GSW0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

9.13.13 Port P6 (P6.7) Input/Output With Schmitt Trigger

Figure 9-15 shows the port diagram. Table 9-28 summarizes the selection of the port function.

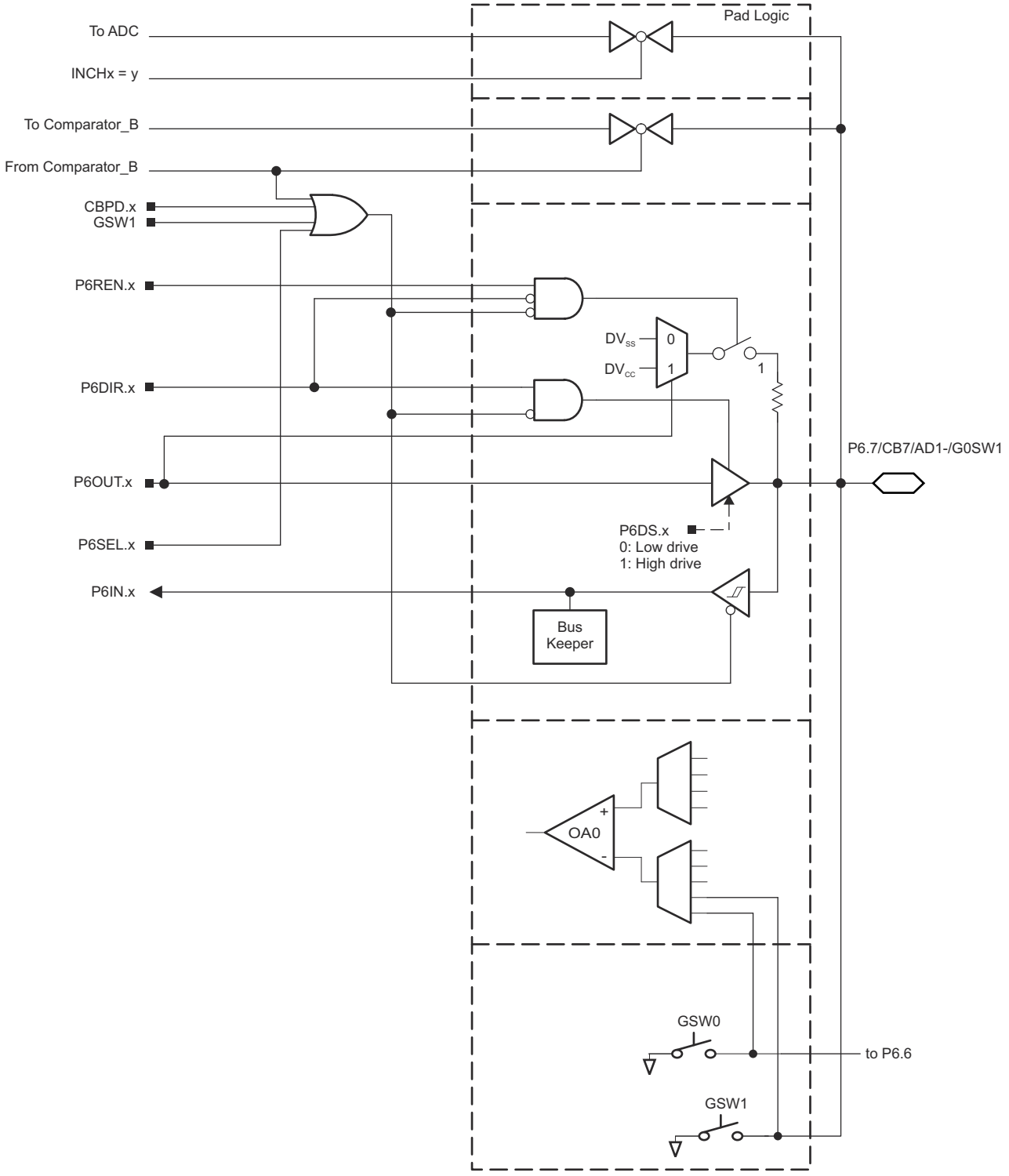


Figure 9-15. Port P6 (P6.7) Diagram

Table 9-28. Port P6 (P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P6SEL.x(3)	CBPD.x(3)	GSW1(3)
P6.7/CB7/AD1-/G0SW1	7	P6.7 (I/O)	I: 0; O: 1	0	0	0
		CB7	X	X	1	0
		AD1- (2)	X	1	X	0
		G0SW1(3)	X	X	X	1

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

9.13.14 Port P7 (P7.2 and P7.3) Input/Output With Schmitt Trigger

Figure 9-16 and Figure 9-17 show the port diagrams. Table 9-29 summarizes the selection of the port function.

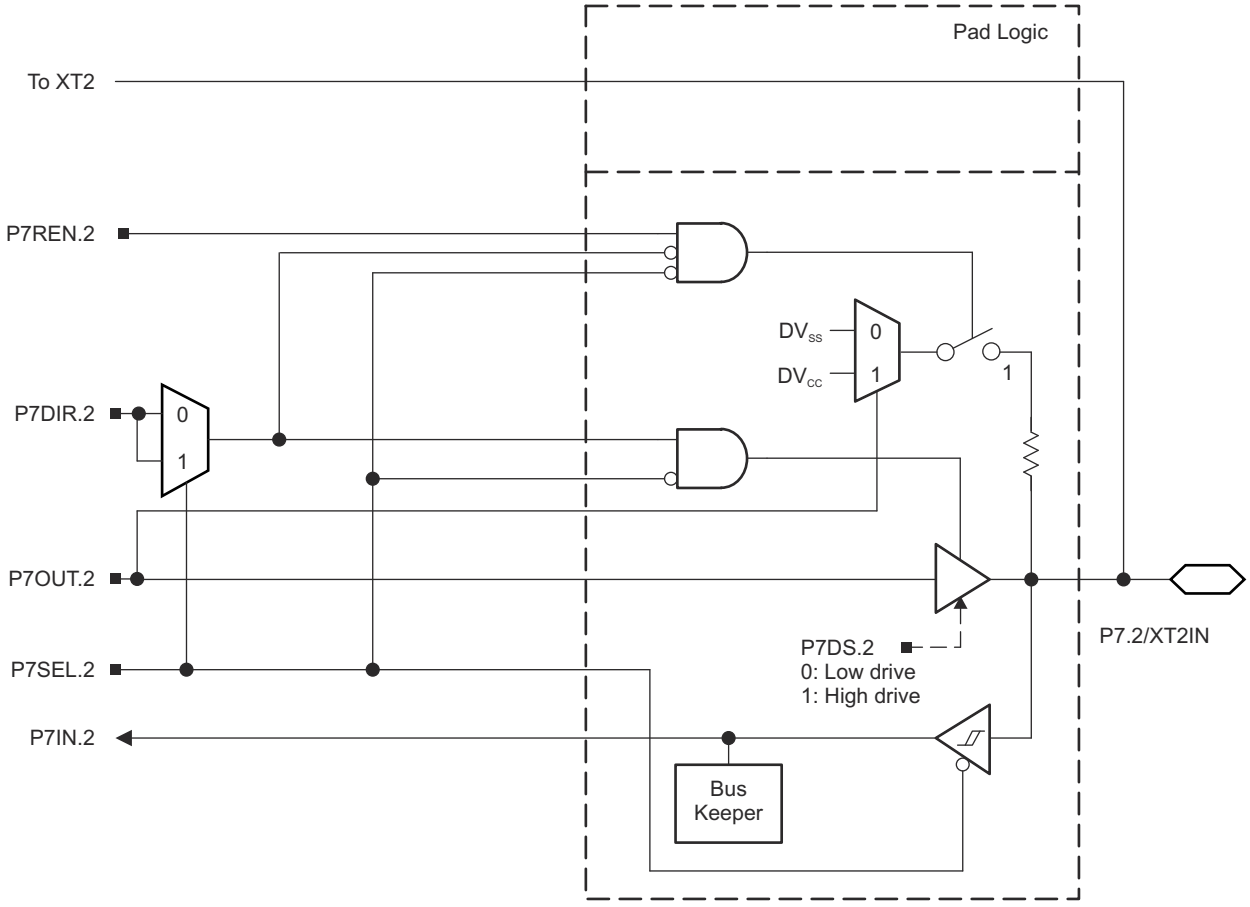


Figure 9-16. Port P7 (P7.2) Diagram

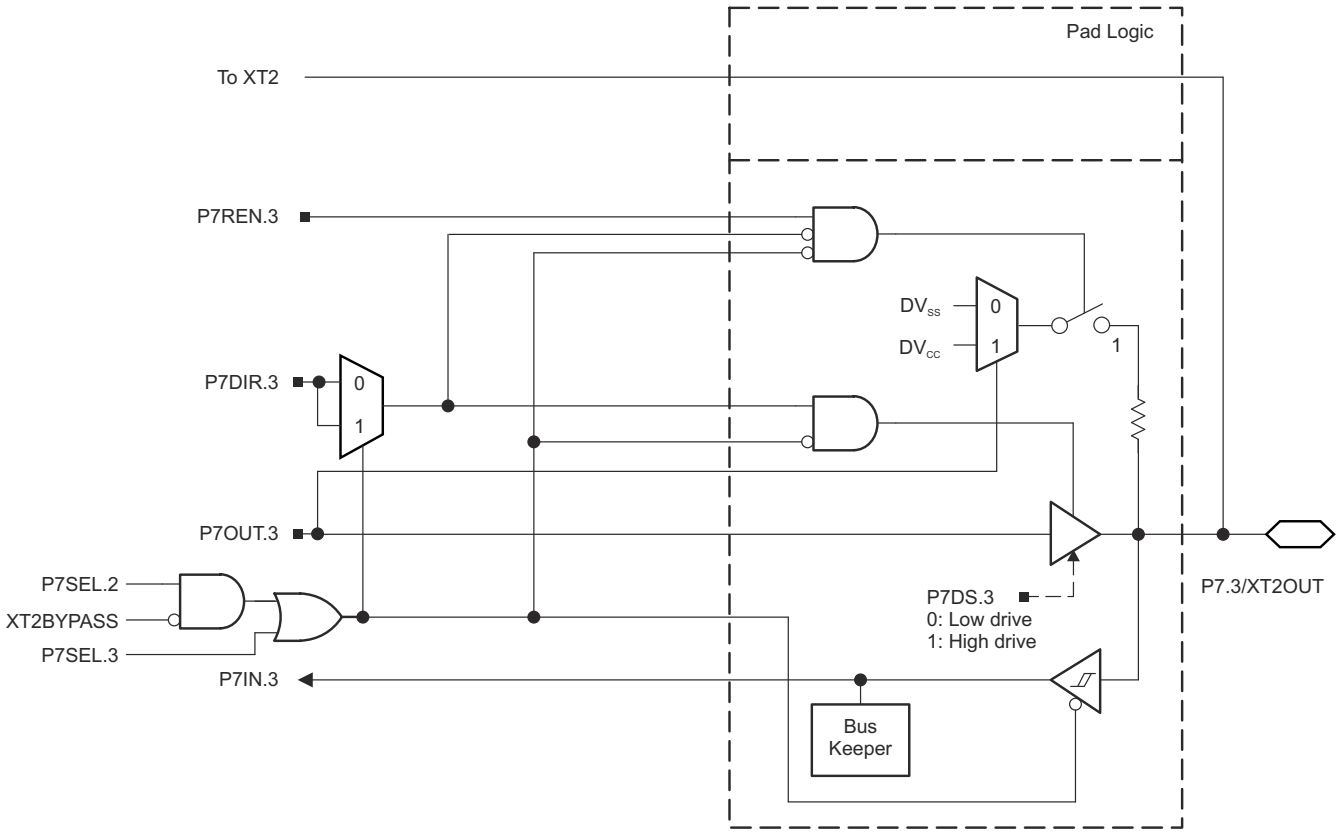


Figure 9-17. Port P7 (P7.3) Diagram

Table 9-29. Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL.2	P7SEL.3	XT2BYPASS
P7.2/XT2IN	2	P7.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P7.3/XT2OUT	3	P7.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode(3)	X	1	X	0
		P7.3 (I/O)(3)	X	1	X	1

(1) X= Don't care
(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.

9.13.15 Port P7 (P7.4) Input/Output With Schmitt Trigger

Figure 9-18 shows the port diagram. Table 9-30 summarizes the selection of the port function.

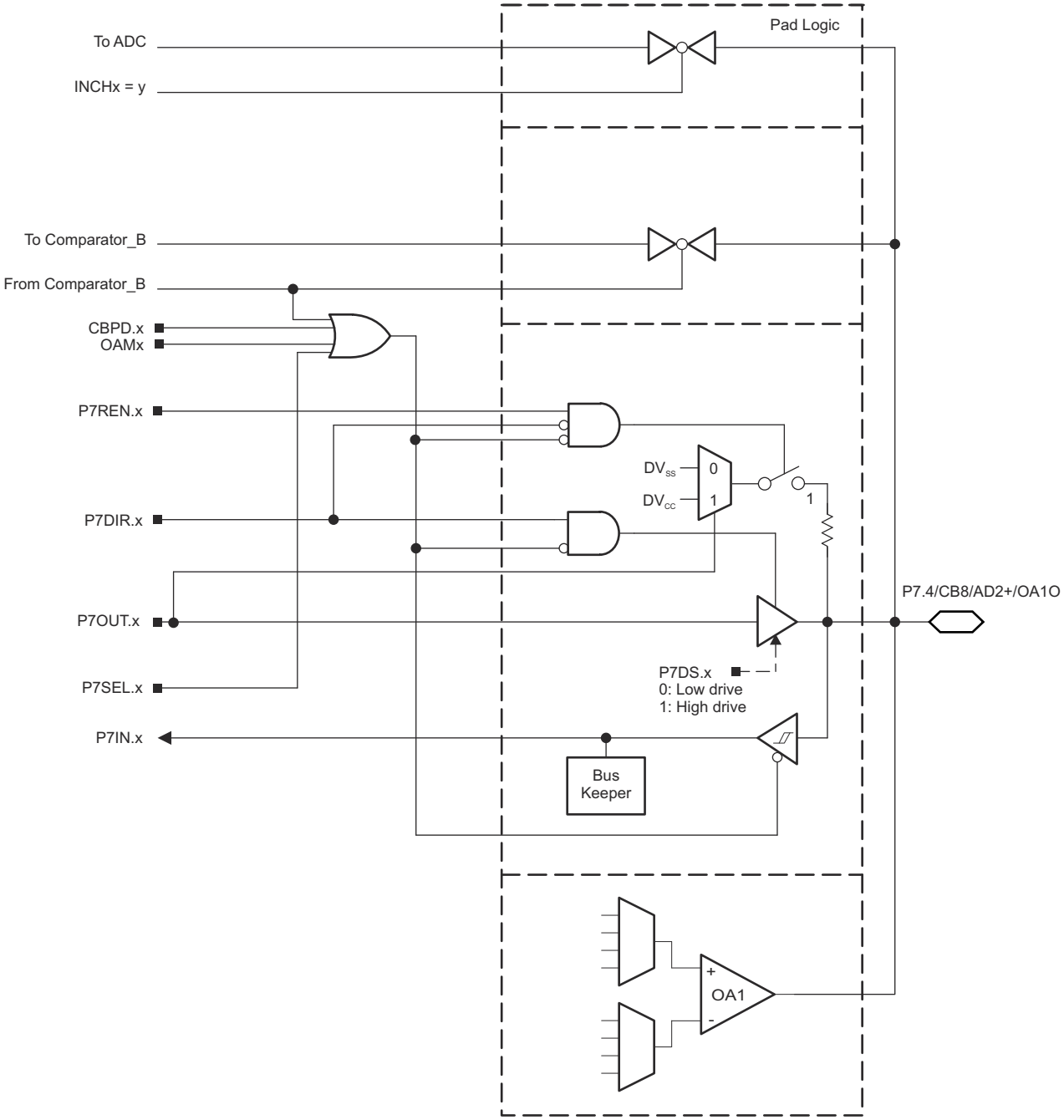


Figure 9-18. Port P7 (P7.4) Diagram

Table 9-30. Port P7 (P7.4) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P7SEL.x(3)	CBPD.x(3)	OAMx(3)
P7.4/CB8/AD2+/OA1O	4	P7.4 (I/O)	I: 0; O: 1	0	0	0(3)
		CB8	X	X	1	0(3)
		AD2+ (2)	X	1	X	0(3)
		OA1O	X	X	X	1(3)

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the output voltage of the amplifier.

9.13.16 Port P7 (P7.5) Input/Output With Schmitt Trigger

Figure 9-19 shows the port diagram. Table 9-31 summarizes the selection of the port function.

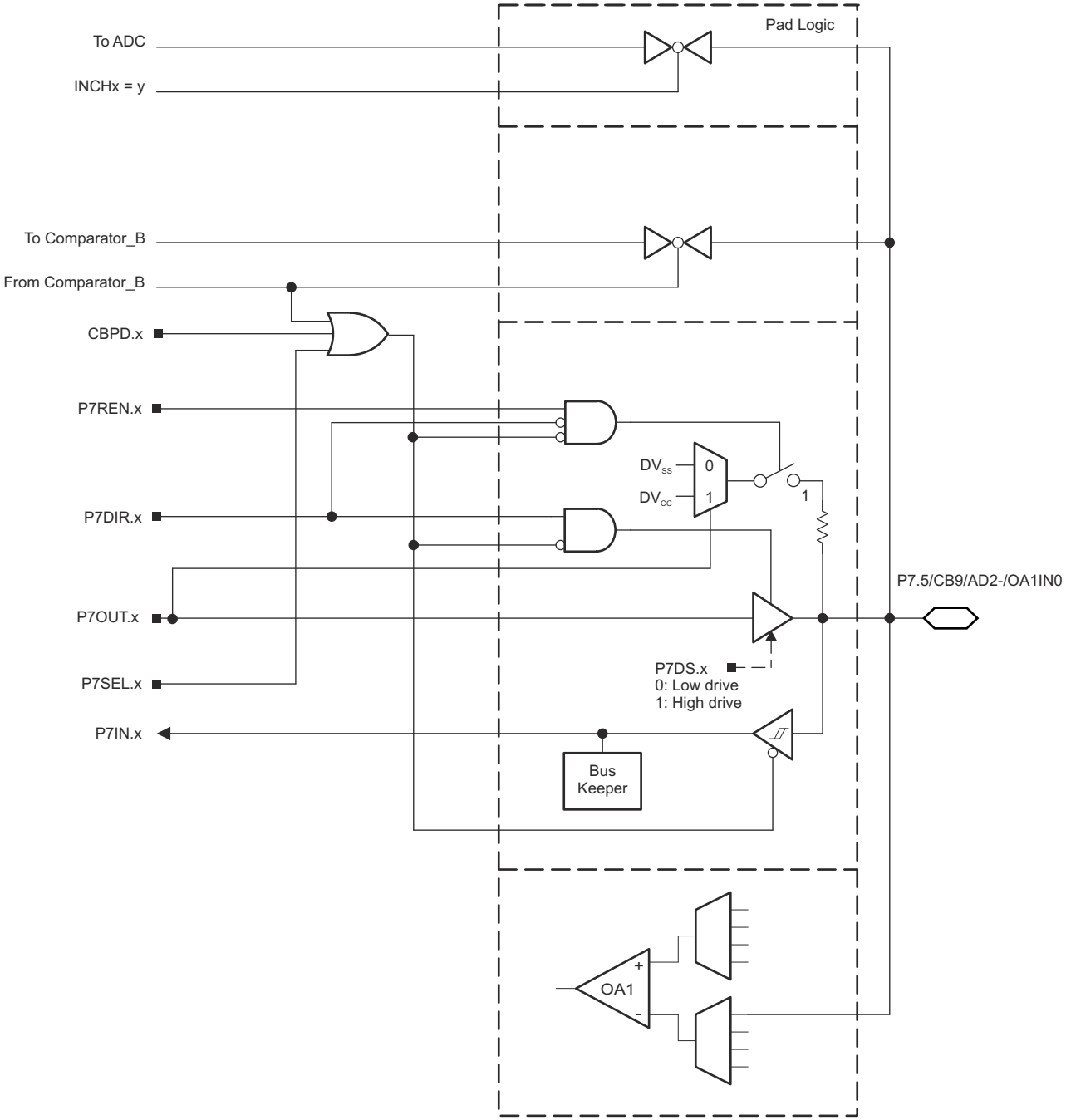


Figure 9-19. Port P7 (P7.5) Diagram

Table 9-31. Port P7 (P7.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P7DIR.x	P7SEL.x(3)	CBPD.x(3)
P7.5/CB9/AD2-/OAIN0	5	P7.5 (I/O)	I: 0; O: 1	0	0
		CB9	X	X	1
		AD2- (2)	X	1	X
		OAIN0(3)	X	1	X

(1) X = Don't care
(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
(3) Setting the P7SEL.x bit or the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

9.13.17 Port P7 (P7.6) Input/Output With Schmitt Trigger

Figure 9-20 shows the port diagram. Table 9-32 summarizes the selection of the port function.

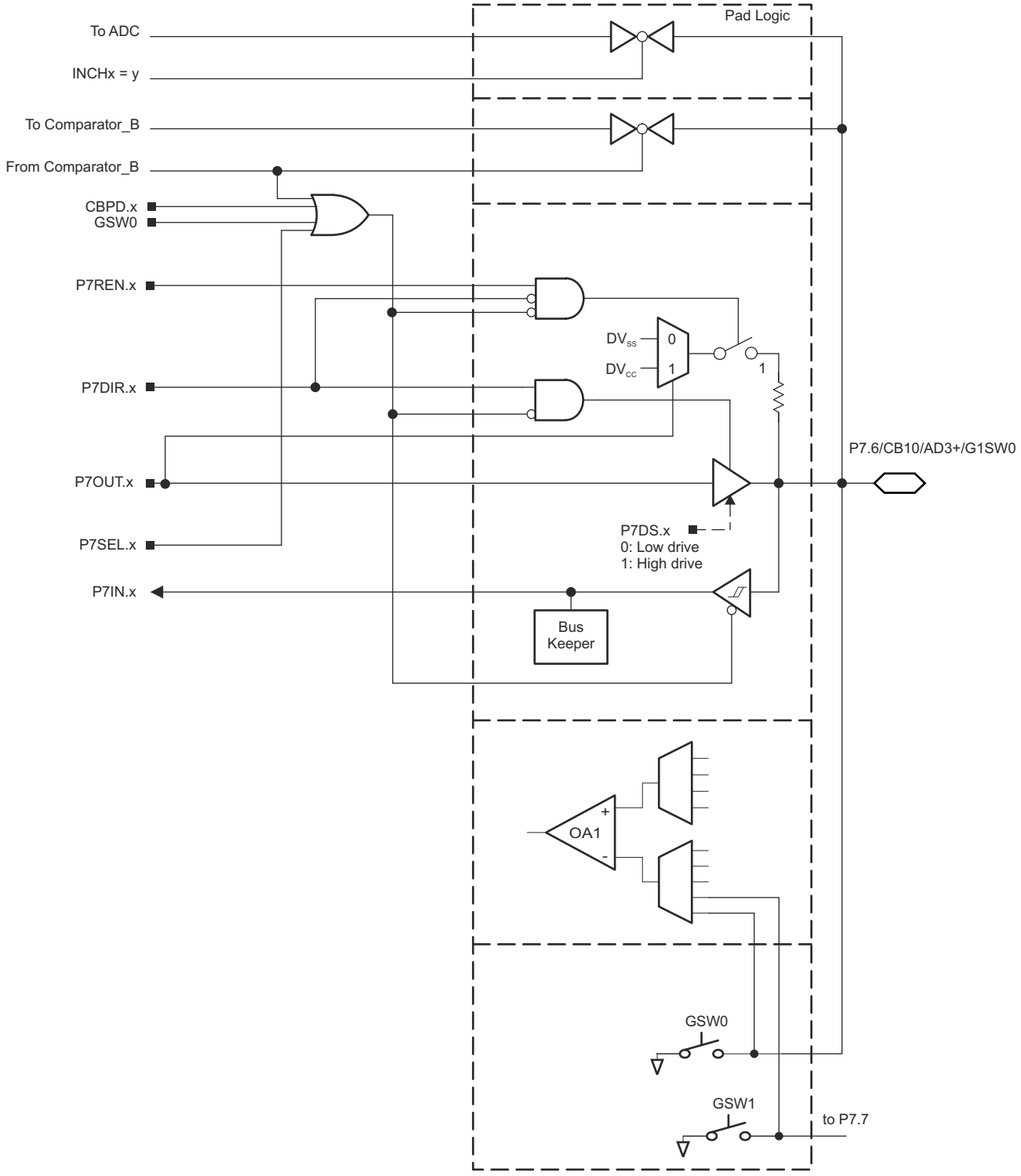


Figure 9-20. Port P7 (P7.6) Diagram

Table 9-32. Port P7 (P7.6) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P7SEL.x(3)	CBPD.x(3)	GSW0(3)
P7.6/CB10/AD3+/G1SW0	6	P7.6 (I/O)	I: 0; O: 1	0	0	0
		CB10	X	X	1	0
		AD3+ (2)	X	1	X	0
		G1SW0(4)	X	X	X	1

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW0 disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

9.13.18 Port P7 (P7.7) Input/Output With Schmitt Trigger

Figure 9-21 shows the port diagram. Table 9-33 summarizes the selection of the port function.

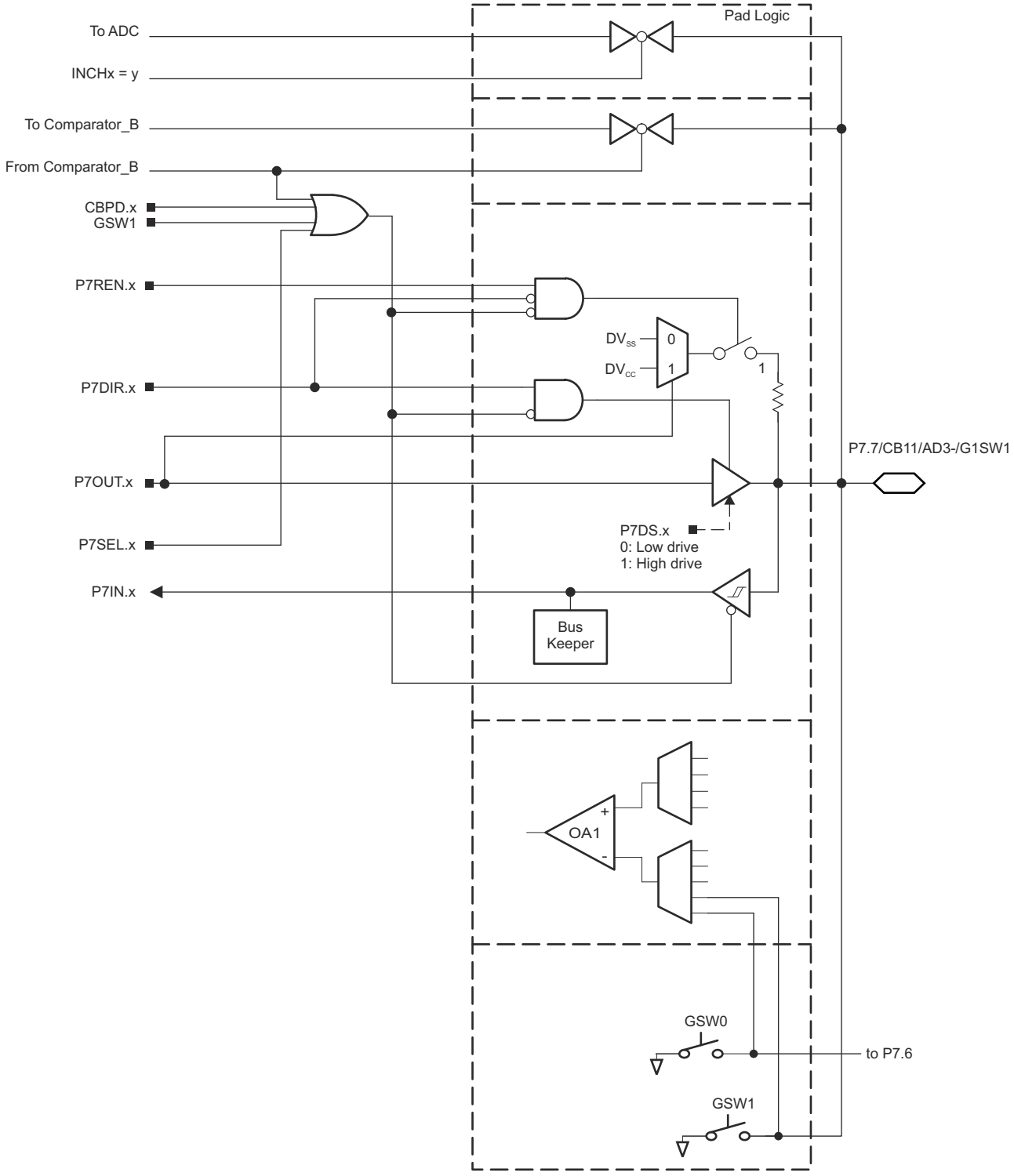


Figure 9-21. Port P7 (P7.7) Diagram

Table 9-33. Port P7 (P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P7SEL.x(3)	CBPD.x(3)	GSW1(3)
P7.7/CB11/AD3-/G1SW1	7	P7.7 (I/O)	I: 0; O: 1	0	0	0
		CB11	X	X	1	0
		AD3- (2)	X	1	X	0
		G1SW1(4)	X	X	X	1

(1) X = Don't care

(2) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(3) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

9.13.19 Port P8 (P8.0 to P8.7) Input/Output With Schmitt Trigger

Figure 9-22 shows the port diagram. Table 9-34 summarizes the selection of the port function.

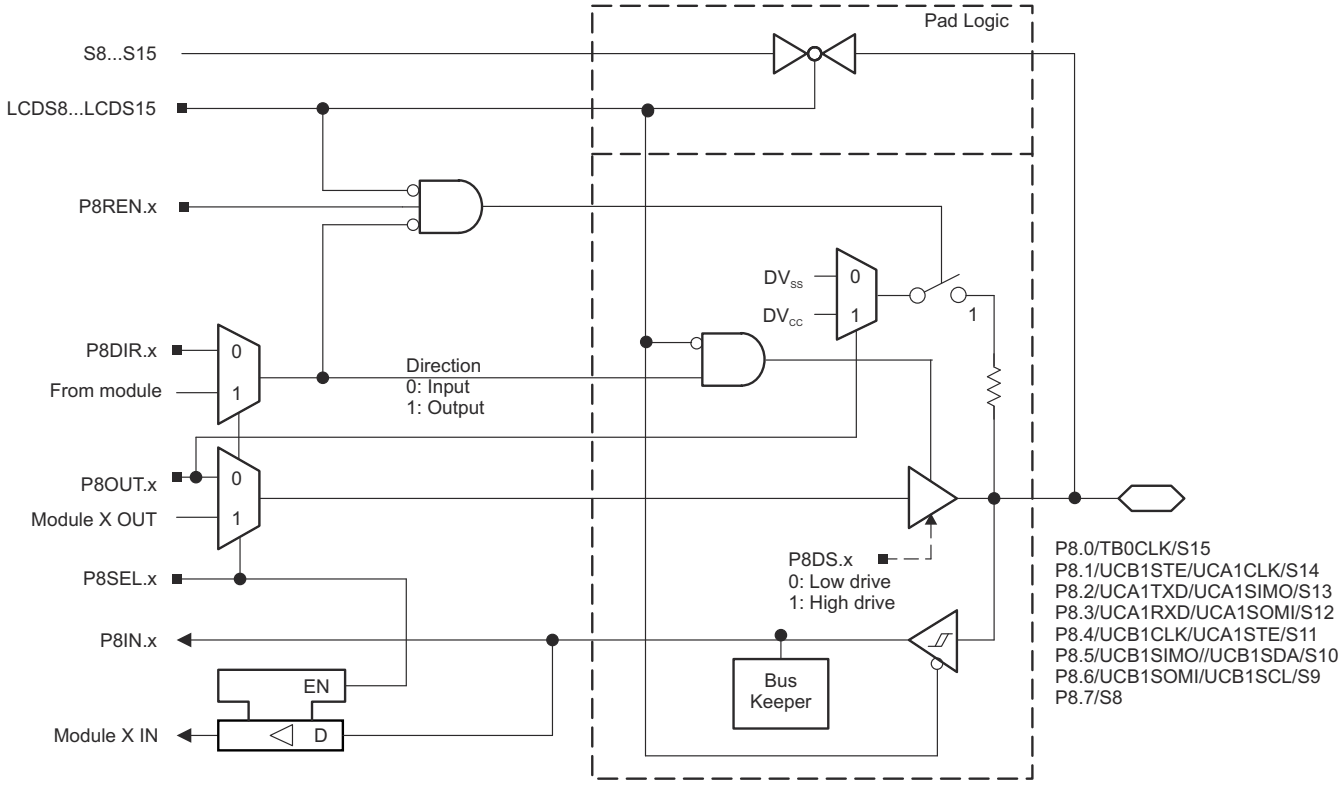


Figure 9-22. Port P8 (P8.0 to P8.7) Diagram

Table 9-34. Port P8 (P8.0 to P8.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P8DIR.x	P8SEL.x	LCDS8 to 16
P8.0/TB0CLK/S15	0	P8.0 (I/O)	I: 0; O: 1	0	0
		Timer TB0.TB0CLK clock input	0	1	0
		S15	X	X	1
P8.1/UCB1STE/UCA1CLK/S14	1	P8.1 (I/O)	I: 0; O: 1	0	0
		UCB1STE/UCA1CLK	X	1	0
		S14	X	X	1
P8.2/UCA1TXD/UCA1SIMO/S13	2	P8.2 (I/O)	I: 0; O: 1	0	0
		UCA1TXD/UCA1SIMO	X	1	0
		S13	X	X	1
P8.3/UCA1RXD/UCA1SOMI/S12	3	P8.3 (I/O)	I: 0; O: 1	0	0
		UCA1RXD/UCA1SOMI	X	1	0
		S12	X	X	1
P8.4/UCB1CLK/UCA1STE/S11	4	P8.4 (I/O)	I: 0; O: 1	0	0
		UCB1CLK/UCA1STE	X	1	0
		S11	X	X	1
P8.5/UCB1SIMO/UCB1SDA/S10	5	P8.5 (I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X	1	0
		S10	X	X	1
P8.6/UCB1SOMI/UCB1SCL/S9	6	P8.6 (I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X	1	0
		S9	X	X	1
P8.7/S8	7	P8.7 (I/O)	I: 0; O: 1	0	0
		S8	X	X	1

(1) X= don't care

9.13.20 Port P9 (P9.0 to P9.7) Input/Output With Schmitt Trigger

Figure 9-23 shows the port diagram. Table 9-35 summarizes the selection of the port function.

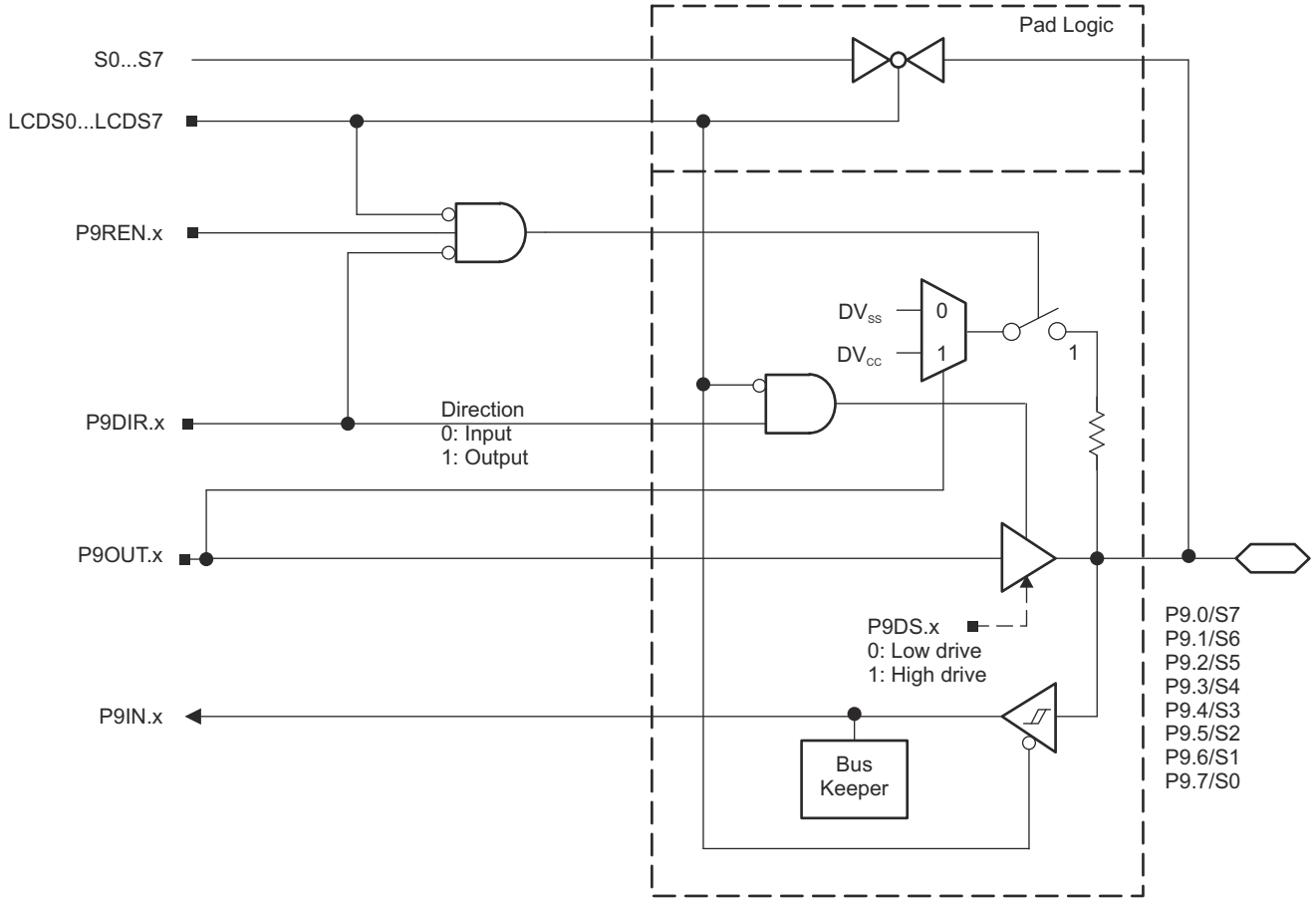


Figure 9-23. Port P9 (P9.0 to P9.7) Diagram

Table 9-35. Port P9 (P9.0 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P9DIR.x	P9SEL.x	LCDS0 to LCDS7
P9.0/S7	0	P9.0 (I/O)	I: 0; O: 1	0	0
		S7	X	X	1
P9.1/S6	1	P9.1 (I/O)	I: 0; O: 1	0	0
		S6	X	X	1
P9.2/S5	2	P9.2 (I/O)	I: 0; O: 1	0	0
		S5	X	X	1
P9.3/S4	3	P9.3 (I/O)	I: 0; O: 1	0	0
		S4	X	X	1
P9.4/S3	4	P9.4 (I/O)	I: 0; O: 1	0	0
		S3	X	X	1
P9.5/S2	5	P9.5 (I/O)	I: 0; O: 1	0	0
		S2	X	X	1
P9.6/S1	6	P9.6 (I/O)	I: 0; O: 1	0	0
		S1	X	X	1
P9.7/S0	7	P9.7 (I/O)	I: 0; O: 1	0	0
		S0	X	X	1

(1) X= don't care

9.13.21 Port U (PU.0/DP, PU.1/DM, PUR) USB Ports for MSP430FG662x

Figure 9-24 shows the port diagram. Table 9-36 and Table 9-37 summarize the port function selection.

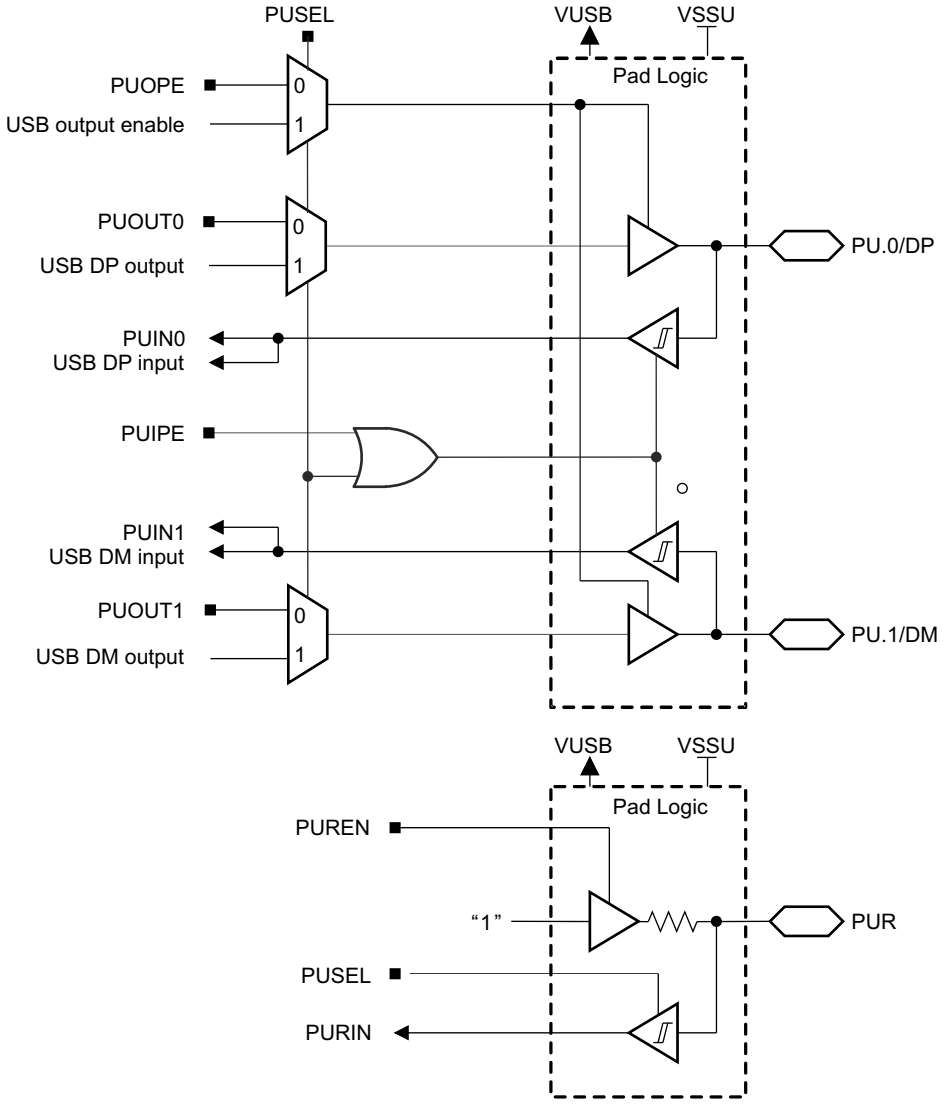


Figure 9-24. Port U (PU.0 and PU.1) Diagram

Table 9-36. Port U (PU.0/DP, PU.1/DM) Output Functions for MSP430FG662x

CONTROL BITS				PIN NAME		FUNCTION
PUSEL	PUDIR	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP	
0	0	X	X	Hi-Z	Hi-Z	Outputs off
0	1	0	0	0	0	Outputs enabled
0	1	0	1	0	1	Outputs enabled
0	1	1	0	1	0	Outputs enabled
0	1	1	1	1	1	Outputs enabled
1	X	X	X	DM	DP	Direction set by USB module

Table 9-37. Port U (PUR) Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pullup disabled
0	1	Input disabled Pullup enabled
1	0	Input enabled Pullup disabled
1	1	Input enabled Pullup enabled

9.13.22 Port J (J.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 9-25 shows the port diagram. Table 9-38 summarizes the selection of the port function.

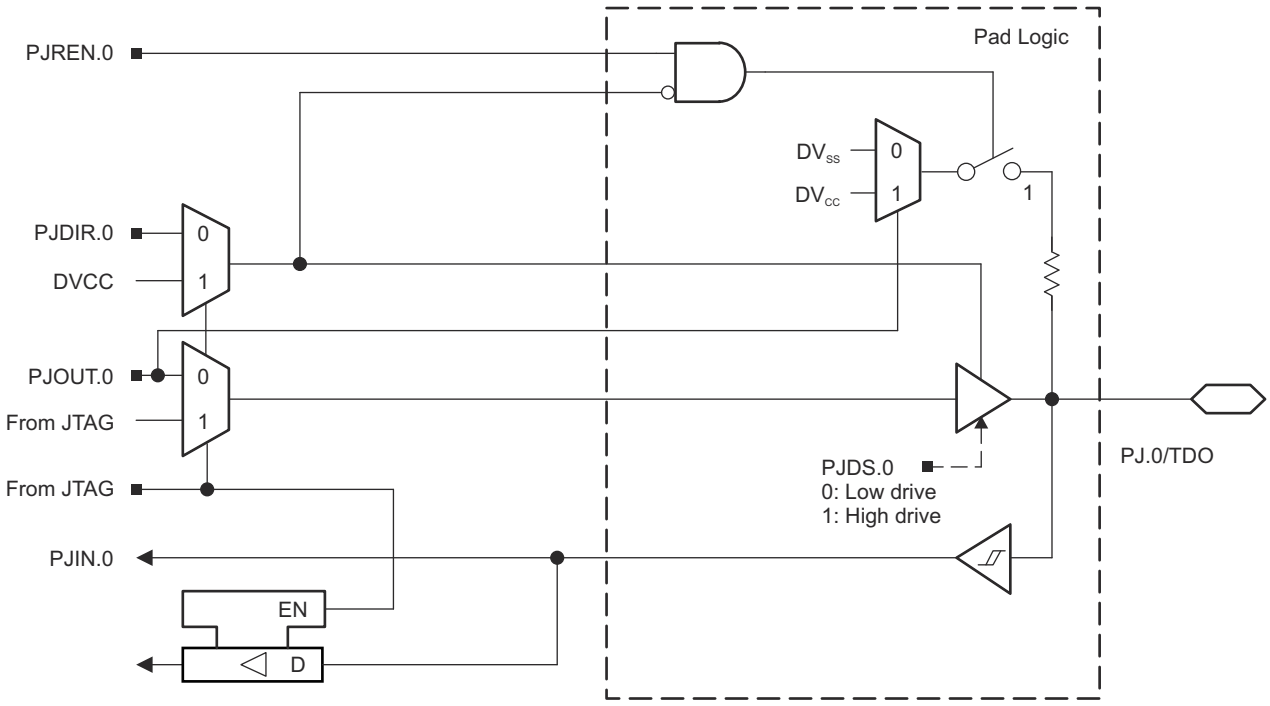


Figure 9-25. Port PJ (PJ.0) Diagram

9.13.23 Port J (J.1 to J.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 9-26 shows the port diagram. Table 9-38 summarizes the selection of the port function.

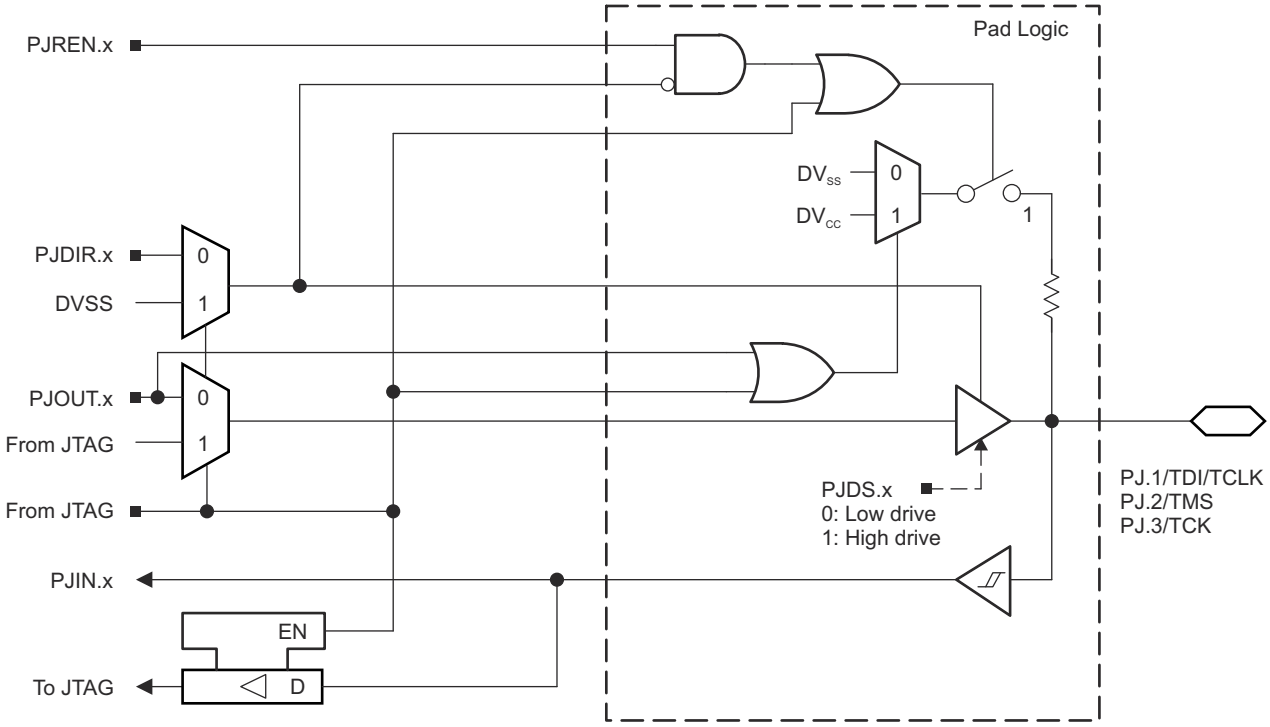


Figure 9-26. Port PJ (PJ.1 to PJ.3) Diagram

Table 9-38. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)(2)	I: 0; O: 1
		TDO(3)	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)(2)	I: 0; O: 1
		TDI/TCLK(3) (4)	X
PJ.2/TMS	2	PJ.2 (I/O)(2)	I: 0; O: 1
		TMS(3) (4)	X
PJ.3/TCK	3	PJ.3 (I/O)(2)	I: 0; O: 1
		TCK(3) (4)	X

(1) X= don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

9.14 Device Descriptors

Table 9-39 summarizes the contents of the device descriptor tag-length-value (TLV) structure.

Table 9-39. Device Descriptor Table

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE			
				FG6626	FG6625	FG6426	FG6425
Info Block	Info length	01A00h	1	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	2	8234h	8235h	8236h	8237h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit
CTSD16 Calibration	CTSD16 calibration tag	01A14h	1	1Dh	1Dh	1Dh	1Dh
	CTSD16 calibration length	01A15h	1	0Ch	0Ch	0Ch	0Ch
	CTSD16 gain factor gain = 1	01A16h	2	Per unit	Per unit	Per unit	Per unit
	CTSD16 gain factor gain = 16	01A18h	2	Per unit	Per unit	Per unit	Per unit
	CTSD16 offset gain = 1	01A1Ah	2	Per unit	Per unit	Per unit	Per unit
	CTSD16 offset gain = 16	01A1Ch	2	Per unit	Per unit	Per unit	Per unit
	CTSD16 internal reference temperature sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit	Per unit
	CTSD16 internal reference temperature sensor 85°C	01A20h	2	Per unit	Per unit	Per unit	Per unit

9.15 Memory

Table 9-40 summarizes the memory organization for all devices.

Table 9-40. Memory Organization

		VALUE(1) (2)			
		MSP430FG6626	MSP430FG6625	MSP430FG6426	MSP430FG6425
Memory (flash) Main: interrupt vector	Total Size	128KB 00FFFFh to 00FF80h	64KB 00FFFFh to 00FF80h	128KB 00FFFFh to 00FF80h	64KB 00FFFFh to 00FF80h
Main: code memory	Bank 3	32KB 0243FFh to 01C400h	NA	32KB 0243FFh to 01C400h	NA
	Bank 2	32KB 01C3FFh to 014400h	NA	32KB 01C3FFh to 014400h	NA
	Bank 1	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h
	Bank 0	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h
RAM	Sector 3	2KB 0043FFh to 003C00h	2KB 0043FFh to 003C00h	2KB 0043FFh to 003C00h	2KB 0043FFh to 003C00h
	Sector 2	2KB 003BFFh to 003400h	2KB 003BFFh to 003400h	2KB 003BFFh to 003400h	2KB 003BFFh to 003400h
	Sector 1	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h

Table 9-40. Memory Organization (continued)

		VALUE(1) (2)			
		MSP430FG6626	MSP430FG6625	MSP430FG6426	MSP430FG6425
	Sector 0	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h
RAM(3)	Sector 7	NA	NA	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h
USB RAM(4)	Sector 7	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	NA	NA
TI factory memory (ROM)	A	128 bytes 001BFFh to 001B80h	128 bytes 001BFFh to 001B80h	128 bytes 001BFFh to 001B80h	128 bytes 001BFFh to 001B80h
	B	128 bytes 001B7Fh to 001B00h	128 bytes 001B7Fh to 001B00h	128 bytes 001B7Fh to 001B00h	128 bytes 001B7Fh to 001B00h
	C	128 bytes 001AFFh to 001A80h	128 bytes 001AFFh to 001A80h	128 bytes 001AFFh to 001A80h	128 bytes 001AFFh to 001A80h
	D	128 bytes 001A7Fh to 001A00h	128 bytes 001A7Fh to 001A00h	128 bytes 001A7Fh to 001A00h	128 bytes 001A7Fh to 001A00h
Information memory (flash)	Info A	128 bytes 0019FFh to 001980h	128 bytes 0019FFh to 001980h	128 bytes 0019FFh to 001980h	128 bytes 0019FFh to 001980h
	Info B	128 bytes 00197Fh to 001900h	128 bytes 00197Fh to 001900h	128 bytes 00197Fh to 001900h	128 bytes 00197Fh to 001900h
	Info C	128 bytes 0018FFh to 001880h	128 bytes 0018FFh to 001880h	128 bytes 0018FFh to 001880h	128 bytes 0018FFh to 001880h
	Info D	128 bytes 00187Fh to 001800h	128 bytes 00187Fh to 001800h	128 bytes 00187Fh to 001800h	128 bytes 00187Fh to 001800h
Bootloader (BSL) memory (flash)	BSL 3	512 bytes 0017FFh to 001600h	512 bytes 0017FFh to 001600h	512 bytes 0017FFh to 001600h	512 bytes 0017FFh to 001600h
	BSL 2	512 bytes 0015FFh to 001400h	512 bytes 0015FFh to 001400h	512 bytes 0015FFh to 001400h	512 bytes 0015FFh to 001400h
	BSL 1	512 bytes 0013FFh to 001200h	512 bytes 0013FFh to 001200h	512 bytes 0013FFh to 001200h	512 bytes 0013FFh to 001200h
	BSL 0	512 bytes 0011FFh to 001000h	512 bytes 0011FFh to 001000h	512 bytes 0011FFh to 001000h	512 bytes 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 000000h	4KB 000FFFh to 000000h	4KB 000FFFh to 000000h	4KB 000FFFh to 000000h

(1) N/A = Not available.
(2) Backup RAM is accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.
(3) Only available on FG642x.
(4) Only available on FG662x. USB RAM can be used as general-purpose RAM when not used for USB operation.

9.15.1 Peripheral File Map

Table 9-41 lists all of the the available peripherals and their base addresses. Table 9-42 through Table 9-78 list the registers and their offset addresses for each peripheral.

Table 9-41. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE(1)
Special Functions (see Table 9-42)	0100h	000h to 01Fh
PMM (see Table 9-43)	0120h	000h to 010h
Flash Control (see Table 9-44)	0140h	000h to 00Fh
CRC16 (see Table 9-45)	0150h	000h to 007h
RAM Control (see Table 9-46)	0158h	000h to 001h
Watchdog (see Table 9-47)	015Ch	000h to 001h
UCS (see Table 9-48)	0160h	000h to 01Fh

Table 9-41. Peripherals (continued)

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE(1)
SYS (see Table 9-49)	0180h	000h to 01Fh
Shared Reference (see Table 9-50)	01B0h	000h to 001h
Port Mapping Control (see Table 9-51)	01C0h	000h to 003h
Port Mapping Port P2 (see Table 9-51)	01D0h	000h to 007h
Port P1, P2 (see Table 9-52)	0200h	000h to 01Fh
Port P3, P4 (see Table 9-53)	0220h	000h to 01Fh
Port P5, P6 (see Table 9-54)	0240h	000h to 00Bh
Port P7, P8 (see Table 9-55)	0260h	000h to 00Bh
Port P9 (see Table 9-56)	0280h	000h to 00Bh
Port PJ (see Table 9-57)	0320h	000h to 01Fh
Timer TA0 (see Table 9-58)	0340h	000h to 02Eh
Timer TA1 (see Table 9-59)	0380h	000h to 02Eh
Timer TB0 (see Table 9-60)	03C0h	000h to 02Eh
Timer TA2 (see Table 9-61)	0400h	000h to 02Eh
Battery Backup (see Table 9-62)	0480h	000h to 01Fh
RTC_B (see Table 9-63)	04A0h	000h to 01Fh
32-Bit Hardware Multiplier (see Table 9-64)	04C0h	000h to 02Fh
DMA General Control (see Table 9-65)	0500h	000h to 00Fh
DMA Channel 0 (see Table 9-65)	0510h	000h to 00Ah
DMA Channel 1 (see Table 9-65)	0520h	000h to 00Ah
DMA Channel 2 (see Table 9-65)	0530h	000h to 00Ah
DMA Channel 3 (see Table 9-65)	0540h	000h to 00Ah
DMA Channel 4 (see Table 9-65)	0550h	000h to 00Ah
DMA Channel 5 (see Table 9-65)	0560h	000h to 00Ah
USCI_A0 (see Table 9-66)	05C0h	000h to 01Fh
USCI_B0 (see Table 9-67)	05E0h	000h to 01Fh
USCI_A1 (see Table 9-68)	0600h	000h to 01Fh
USCI_B1 (see Table 9-69)	0620h	000h to 01Fh
DAC12_A (see Table 9-70)	0780h	000h to 01Fh
Comparator_B (see Table 9-71)	08C0h	000h to 00Fh
USB configuration (see Table 9-72)(2)	0900h	000h to 014h
USB control (see Table 9-73)(2)	0920h	000h to 01Fh
LDO-PWR; LDO and Port U configuration (see Table 9-74) (3)	0900h	000h to 014h
LCD_B control (see Table 9-75)	0A00h	000h to 05Fh
CTSD16 (see Table 9-76)	0A80h	000h to 05Fh
OA0 and GSW0 (see Table 9-77)	0AE0h	000h to 00Fh
OA1 and GSW1 (see Table 9-78)	0AF0h	000h to 00Fh

(1) For a detailed description of the individual control register offset addresses, see the MSP430F5xx and MSP430F6xx Family User's Guide.
(2) Only on devices with peripheral module USB.
(3) Only on devices with peripheral module LDO-PWR.

Table 9-42. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 9-43. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 9-44. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 9-45. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC result	CRC16INIRES	04h

Table 9-46. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 9-47. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 9-48. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 9-49. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 9-50. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 9-51. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P2: 01D0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password	PMAPPWD	00h
Port mapping control	PMAPCTL	02h
Port P2.0 mapping	P2MAP0	00h
Port P2.1 mapping	P2MAP1	01h
Port P2.2 mapping	P2MAP2	02h
Port P2.3 mapping	P2MAP3	03h
Port P2.4 mapping	P2MAP4	04h
Port P2.5 mapping	P2MAP5	05h
Port P2.6 mapping	P2MAP6	06h
Port P2.7 mapping	P2MAP7	07h

Table 9-52. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 9-53. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P3 interrupt vector word	P3IV	0Eh
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

Table 9-54. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 9-55. Port P7, P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 resistor enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 resistor enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 9-56. Port P9 Register (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 resistor enable	P9REN	06h
Port P9 drive strength	P9DS	08h
Port P9 selection	P9SEL	0Ah

Table 9-57. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 9-58. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 9-59. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 9-60. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 9-61. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 9-62. Battery Backup Registers (Base Address: 0480h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Battery backup memory 0	BAKMEM0	00h
Battery backup memory 1	BAKMEM1	02h
Battery backup memory 2	BAKMEM2	04h
Battery backup memory 3	BAKMEM3	06h
Battery backup control	BAKCTL	1Ch
Battery charger control	BAKCHCTL	1Eh

Table 9-63. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds	RTCSEC	10h
RTC minutes	RTCMIN	11h
RTC hours	RTCHOUR	12h
RTC day of week	RTCDOW	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion	BIN2BCD	1Ch
BCD-to-binary conversion	BCD2BIN	1Eh

Table 9-64. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 9-65. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA general control: DMA module control 0	DMACTL0	00h
DMA general control: DMA module control 1	DMACTL1	02h
DMA general control: DMA module control 2	DMACTL2	04h
DMA general control: DMA module control 3	DMACTL3	06h
DMA general control: DMA module control 4	DMACTL4	08h
DMA general control: DMA interrupt vector	DMAIV	0Ah
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA channel 3 control	DMA3CTL	00h
DMA channel 3 source address low	DMA3SAL	02h
DMA channel 3 source address high	DMA3SAH	04h
DMA channel 3 destination address low	DMA3DAL	06h
DMA channel 3 destination address high	DMA3DAH	08h
DMA channel 3 transfer size	DMA3SZ	0Ah
DMA channel 4 control	DMA4CTL	00h
DMA channel 4 source address low	DMA4SAL	02h
DMA channel 4 source address high	DMA4SAH	04h
DMA channel 4 destination address low	DMA4DAL	06h
DMA channel 4 destination address high	DMA4DAH	08h
DMA channel 4 transfer size	DMA4SZ	0Ah
DMA channel 5 control	DMA5CTL	00h
DMA channel 5 source address low	DMA5SAL	02h
DMA channel 5 source address high	DMA5SAH	04h
DMA channel 5 destination address low	DMA5DAL	06h
DMA channel 5 destination address high	DMA5DAH	08h
DMA channel 5 transfer size	DMA5SZ	0Ah

Table 9-66. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA0CTL0	00h
USCI control 1	UCA0CTL1	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 9-67. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB0CTL0	00h
USCI synchronous control 1	UCB0CTL1	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 9-68. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA1CTL0	00h
USCI control 1	UCA1CTL1	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 9-69. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB1CTL0	00h
USCI synchronous control 1	UCB1CTL1	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 9-70. DAC12_A Registers (Base Address: 0780h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DAC12_A channel 0 control 0	DAC12_0CTL0	00h
DAC12_A channel 0 control 1	DAC12_0CTL1	02h
DAC12_A channel 0 data	DAC12_0DAT	04h
DAC12_A channel 0 calibration control	DAC12_0CALCTL	06h
DAC12_A channel 0 calibration data	DAC12_0CALDAT	08h
DAC12_A channel 1 control 0	DAC12_1CTL0	10h
DAC12_A channel 1 control 1	DAC12_1CTL1	12h
DAC12_A channel 1 data	DAC12_1DAT	14h
DAC12_A channel 1 calibration control	DAC12_1CALCTL	16h
DAC12_A channel 1 calibration data	DAC12_1CALDAT	18h
DAC12_A interrupt vector word	DAC12IV	1Eh

Table 9-71. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 9-72. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key/ID	USBKEYID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB power voltage setting	USBPWRVSR	0Ah
USB PLL control	USBPLLCTL	10h
USB PLL divider	USBPLLDIV	12h
USB PLL interrupts	USBPLLIR	14h

Table 9-73. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint_0 configuration	USBIEPCNF_0	00h
Input endpoint_0 byte count	USBIEPBCNT_0	01h
Output endpoint_0 configuration	USBOEPCNFG_0	02h
Output endpoint_0 byte count	USBOEPBCNT_0	03h
Input endpoint interrupt enables	USBIEPIE	0Eh
Output endpoint interrupt enables	USBOEPIE	0Fh
Input endpoint interrupt flags	USBIEPIFG	10h
Output endpoint interrupt flags	USBOEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	USBMAINT	16h
Time stamp	USBTSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	USBFUNADR	1Fh

Table 9-74. LDO and Port U Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LDO key and ID	LDOKEYPID	00h
PU port control	PUCTL	04h
LDO power control	LDOPWRCTL	08h

Table 9-75. LCD_B Registers (Base Address: 0A00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_B control 0	LCDBCTL0	000h
LCD_B control 1	LCDBCTL1	002h
LCD_B blinking control	LCDBBLKCTL	004h
LCD_B memory control	LCDBMEMCTL	006h
LCD_B voltage control	LCDBVCTL	008h
LCD_B port control 0	LCDBPCTL0	00Ah
LCD_B port control 1	LCDBPCTL1	00Ch
LCD_B port control 2	LCDBPCTL2	00Eh
LCD_B charge pump control	LCDBCTL0	012h
LCD_B interrupt vector word	LCDBIV	01Eh
LCD_B memory 1	LCDM1	020h
LCD_B memory 2	LCDM2	021h
⋮	⋮	⋮
LCD_B memory 22	LCDM22	035h
LCD_B blinking memory 1	LCDBM1	040h
LCD_B blinking memory 2	LCDBM2	041h
⋮	⋮	⋮
LCD_B blinking memory 22	LCDBM22	055h

Table 9-76. CTSD16 Registers (Base Address: 0A80h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CTSD16 control	CTSD16CTL	00h
CTSD16 channel 0 control	CTSD16CCTL0	02h
CTSD16 channel 0 input control	CTSD16INCTL0	04h
CTSD16 channel 0 preload	CTSD16PRE0	06h
CTSD16 interrupt flag	CTSD16IFG	2Ch
CTSD16 interrupt enable	CTSD16IE	2Eh
CTSD16 interrupt vector	CTSD16IV	30h
CTSD16 channel 0 conversion memory	CTSD16MEM0	32h

Table 9-77. OA0 Registers (Base Address: 0AE0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
OA0 control 0	OA0CTL0	00h
OA0 positive input terminal switches	OA0PSW	02h
OA0 negative input terminal switches	OA0NSW	04h
OA0 ground switches	OA0GSW	0Eh

Table 9-78. OA1 Registers (Base Address: 0AF0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
OA1 control 0	OA1CTL0	00h
OA1 positive input terminal switches	OA1PSW	02h
OA1 negative input terminal switches	OA1NSW	04h
OA1 ground switches	OA1GSW	0Eh

9.16 Identification

9.16.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see Section 11.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in Section 9.14.

9.16.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see Section 11.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in Section 9.14.

9.16.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the MSP430 Programming With the JTAG Interface.

10 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

10.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommend for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

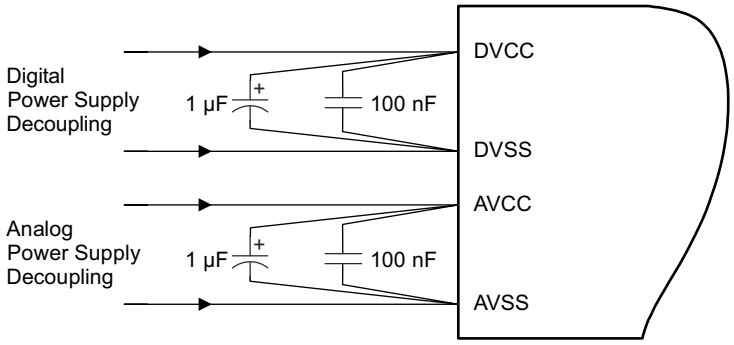


Figure 10-1. Power Supply Decoupling

10.1.2 External Oscillator

Depending on the device variant (see Section 6), the device can support a low-frequency crystal (32 kHz) on the XT1 pins, a high-frequency crystal on the XT2 pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN and XT2IN input pins that meet the specifications of the respective oscillator if the appropriate XT1BYPASS or XT2BYPASS mode is selected. In this case, the associated XOUT and XT2OUT pins can be used for other purposes. If they are left unused, they must be terminated according to Table 7-4.

Figure 10-2 shows a typical connection diagram.

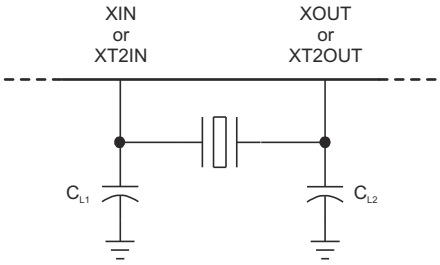


Figure 10-2. Typical Crystal Connection

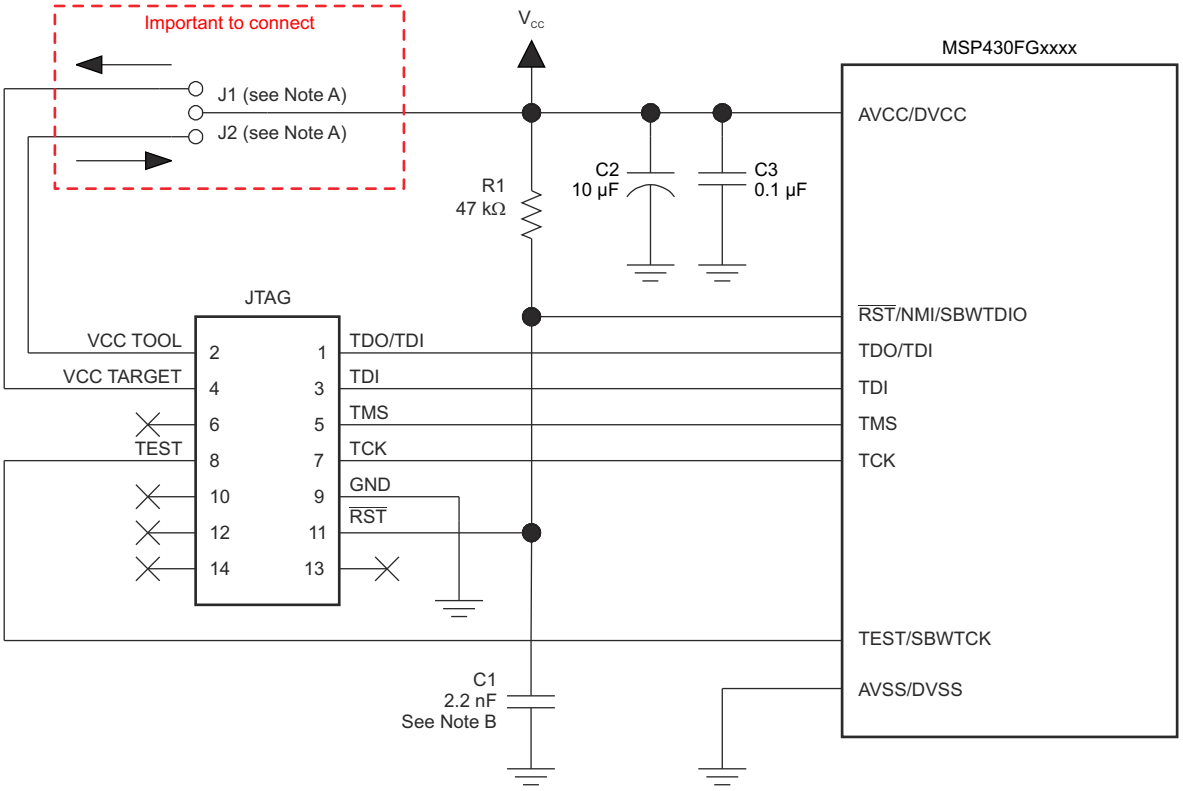
See MSP430 32-kHz Crystal Oscillators for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

10.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 10-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 10-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 10-3 and Figure 10-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

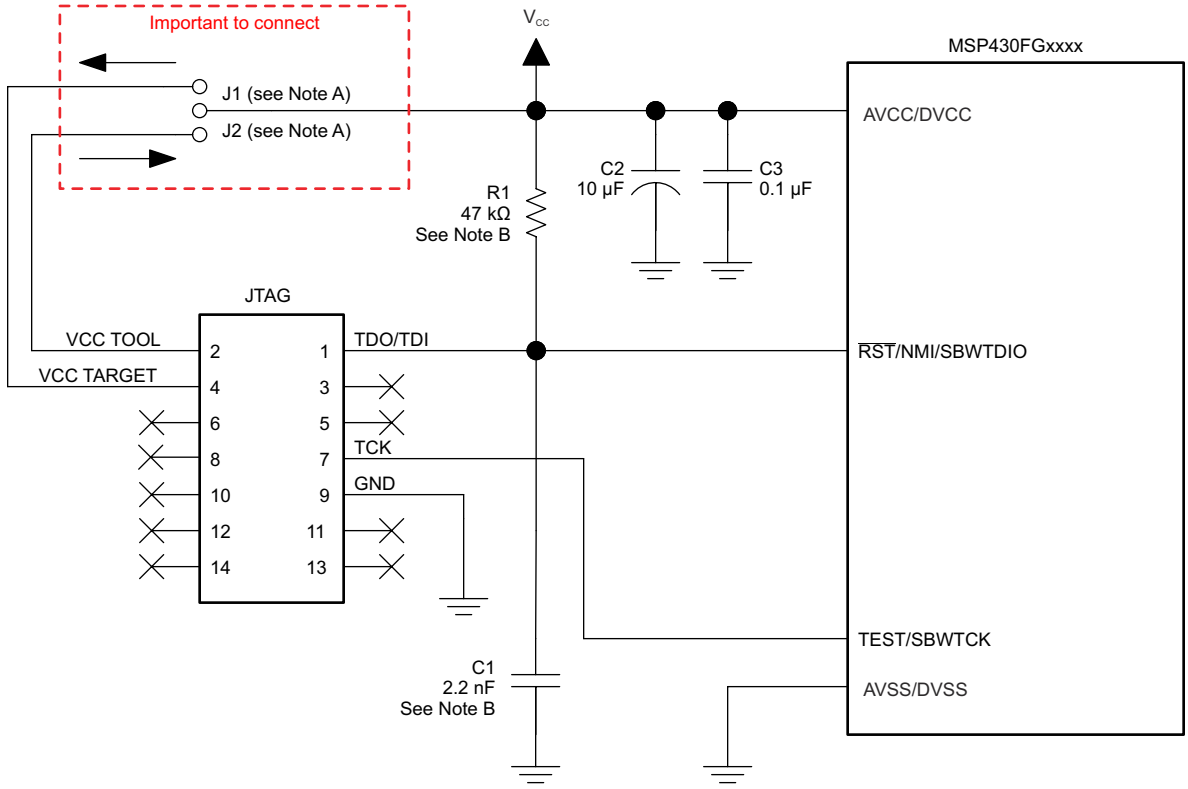
For additional design information regarding the JTAG interface, see the MSP430 Hardware Tools User's Guide.



A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 10-3. Signal Connections for 4-Wire JTAG Communication



A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device RST/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 10-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

10.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the MSP430F5xx and MSP430F6xx Family User's Guide for more information on the referenced control registers and bits.

10.1.5 Unused Pins

For details on the connection of unused pins, see Section 7.6.

10.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See MSP430 32-kHz Crystal Oscillators for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See MSP430 System-Level ESD Considerations for guidelines.

10.1.7 Do's and Don'ts

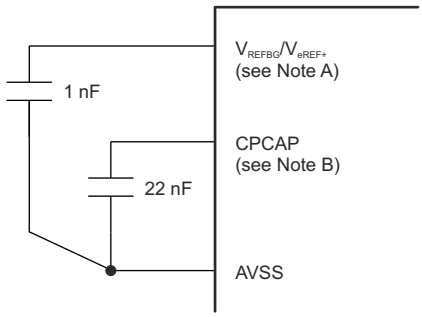
TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Section 8.1*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

10.2 Peripheral- and Interface-Specific Design Information

10.2.1 CTSD16 Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see Section 9.12.16. When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

Solid decoupling on both the digital and analog supplies is also required (best with two capacitors, one 1 µF and one 100 nF [see Section 10.1.1]).

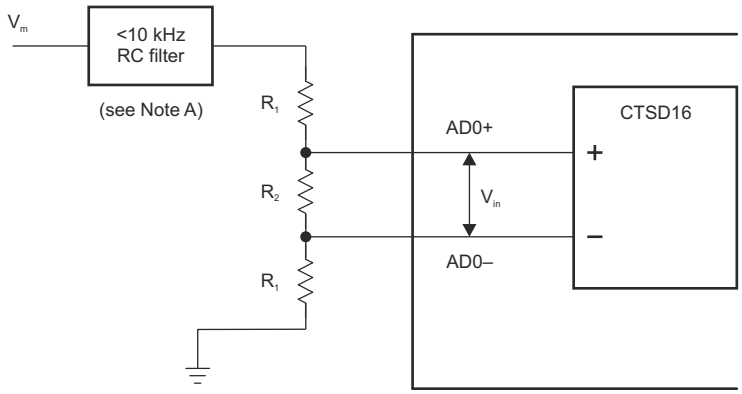


A. The capacitor reduces noise when using internal V_{REFBG} setting. This pin is also used for the external reference input for the CTSD16 or DAC, and when doing so the capacitor is not needed. Because of the shared signal path and pin, the internal and external references (V_{REFBG} and V_{eREF+}, respectively) cannot be used at the same time.

B. The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the CTSD16 or by the OA module. See the register settings for each module in the MSP430F5xx and MSP430F6xx Family User's Guide for enabling this operation.

Figure 10-5. CTSD16 Partial Schematic

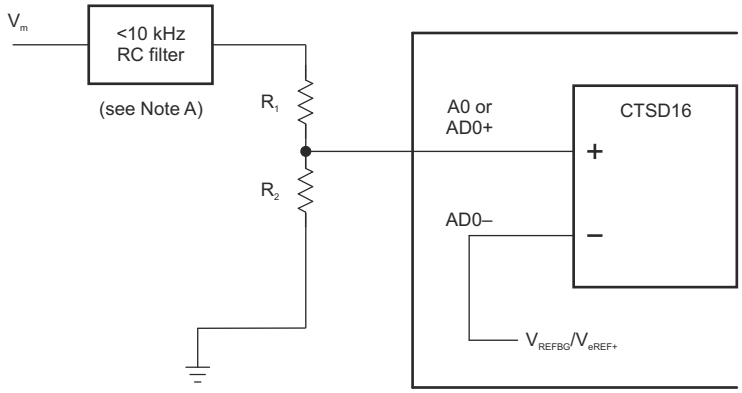
10.2.1.1 Example Measurement Schematic – Differential Input



A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

Figure 10-6. CTSD16 Measurement Schematic – Differential Input

10.2.1.2 Example Measurement Schematic – Single-Ended Input



A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

Figure 10-7. CTSD16 Measurement Schematic – Single-Ended Input

10.2.1.3 Design Requirements

As with any high-resolution ADC, appropriate printed circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. Therefore, solid decoupling on both the digital and analog supplies is required (best with two capacitors, one 1 µF and one 100 nF [see Section 10.1.1]).

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

If the internal reference is used, the reference voltage should be buffered externally by connecting a small (approximately 1 nF) capacitor to the VREFBG pin to reduce the noise on the reference.

The CTSD16 has a fixed 1.024-MHz clock (f_M). Fault flags for this oscillator are described in the CTSD16 and UCS section of the MSP430F5xx and MSP430F6xx Family User's Guide.

Rail-to-rail operation mode is available when the OA module is used to buffer the CTSD16 inputs. For more information, see the CTSD16 and the OA modules in the MSP430F5xx and MSP430F6xx Family User's Guide.

10.2.1.4 Detailed Design Procedure

10.2.1.4.1 OSR and Sampling Frequency

A simple equation guides the relationship between effective sampling frequency and oversampling ratio (OSR) for CTSD16.

$$f_s = \frac{f_m}{OSR} \tag{2}$$

Where

- f_s = effective sampling frequency
- f_m = modulation frequency

For the CTSD16, the modulation frequency is set to 1.024 MHz. Using Equation 2 with an example OSR of 256, the effective sampling frequency would be 4 kHz. The OSR value also affects the number of bits in the digital filter output. See the CTSD16 chapter in the MSP430F5xx and MSP430F6xx Family User's Guide for additional information and available OSR values.

10.2.1.4.2 Differential Input Range Explanation

The following equations can give guidance on the input range for the CTSD16 while using an external reference. Keep in mind the absolute bounds of an external reference as mentioned in the specifications section of this module. The external and internal references cannot be used at the same time, because they share the same signal path and pin. For internal reference ranges, see Section 8.8.11.

$$V_{FSR+} = \frac{+V_R}{GAIN} \tag{3}$$

$$V_{FSR-} = \frac{-V_R}{GAIN} \tag{4}$$

$$\text{Full-Scale Range} = V_{FSR+} - V_{FSR-} = 2 \times \frac{V_R}{GAIN} \tag{5}$$

$$V_{ID} = 0.8\ V_{FSR-} \text{ to } 0.8\ V_{FSR+}, \text{ with externally sourced } V_R \tag{6}$$

Where

- V_{FSR} is the full-scale range voltage
- V_{ID} is the differential input voltage
- V_R is the reference voltage

The differential input voltage range with internal voltage reference at different GAIN settings is given in Section 8.8.11. Using Equation 3 through Equation 6, determine the absolute maximum differential input ranges for the CTSD16 with a given external voltage reference. Equation 7 corresponds to the example circuit in Figure 10-6 and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_2 + 2R_1} \times \frac{1}{1 + \frac{R_{eff}}{2R_{in}}} \tag{7}$$

Where

- $R_{eff} = (R_2 \times 2R_1) / ((R_2 + 2R_1)$
- V_{in} is the differential voltage input to CTSD16
- V_m is the voltage to measure

- R_{in} is the internal resistance of the CTSD16 (see Section 8.8.11)

10.2.1.4.3 Single-Ended Input Mode

The CTSD16 has six single-ended analog inputs and four differential inputs that can be placed in single-ended mode by the CTSDINCHx bits in the CTSD16INCTLx registers. These single-ended modes use the fully differential path of the CTSD16 by internally tying the negative input to the V_{REFBG}/V_{eREF+} signal. This means for the differential inputs in single-ended mode, the external pin normally tied to the negative input can be used for its alternate functions. Equation 8 through Equation 11 apply for full-scale range while in single-ended mode.

$$V_{FSR+} = V_R + \frac{V_R}{GAIN} \tag{8}$$

$$V_{FSR-} = V_R - \frac{V_R}{GAIN} \tag{9}$$

$$\text{Full-Scale Range} = V_{FSR+} - V_{FSR-} = \left(V_R + \frac{V_R}{GAIN}\right) - \left(V_R - \frac{V_R}{GAIN}\right) = 2 \times \frac{V_R}{GAIN} \tag{10}$$

$$V_I = V_R - 0.8 \times \left(\frac{V_R}{GAIN}\right) \text{ to } V_R + 0.8 \times \left(\frac{V_R}{GAIN}\right) \tag{11}$$

Where

- V_{FSR} is the full-scale range voltage
- V_I is the single-ended input voltage range for data-sheet specified performance
- V_R is the reference voltage

To ensure the measured voltage is within the single-ended voltage range, a simple voltage divider circuit can be used to condition the desired input signal. In single-ended mode, additional error may be introduced by noise when compared to a fully differential measurement. Equation 12 corresponds to the example circuit in Figure 10-7 and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_1 + R_2} \tag{12}$$

Where

- V_{in} is the single-ended voltage input to CTSD16
- V_m is the voltage to measure

10.2.1.4.4 Offset Calibration

In some applications, it is necessary to calibrate the module for offset error. This module allows an easy way to do this by providing internal connections from input to VREF or DAC0. To short AD4+ and AD4- to VREF or DAC0, change the CTSD16INCHx setting for each channel to 0x11 for VREF and 0x12 for DAC0. This allows calibration of the CTSD16 input stage by what is measured from the ideal value. The total signal chain offset depends on the impedance of the external circuitry; thus, the actual offset seen at any of the analog inputs may be different.

10.2.1.5 Layout Guidelines

Components that are shown in the partial schematic (see Figure 10-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

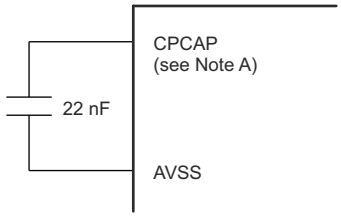
The analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

10.2.2 Operational Amplifier With Ground Switches Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see Section 9.12.16. When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

Solid decoupling on both the digital and analog supplies is also required (best with two capacitors, one 1 µF and one 100 nF [see Section 10.1.1]).

10.2.2.1 Reference Schematic



A. The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the PGA buffers of the CTSD16 or by the OA module. See the register settings for each module in the MSP430F5xx and MSP430F6xx Family User's Guide for enabling this operation.

Figure 10-8. Op Amp Partial Schematic

10.2.2.2 Design Requirements

As with any analog signals, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the signal. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy. For more information about noise and its effects on op amps, see Noise Analysis in Operational Amplifiers.

Rail-to-rail operation mode is available with the OA module at the cost of increased current. This should be used when OA input is near the AVCC rail. See the V_{CM} specification (see Section 8.8.14) to see if rail-to-rail operation is required for your application. For more information, see the OA chapter of the MSP430F5xx and MSP430F6xx Family User's Guide.

Ground switches are also available for use. See Section 9.12.16 for connections. These ground switches provide a low-ohmic connection to ground to both internal connections and to the external pin. When a ground switch is active, the Digital I/O logic for the corresponding pin is ignored.

10.2.2.3 Detailed Design Procedure

Operational amplifiers are a diverse and useful tool in many applications. Some common configurations that might prove to be useful to the user are transimpedance amplifiers to convert currents to voltage, voltage-gain amplifiers, and buffering configurations. For more information about how to design these circuits along with other common configurations, see the following documents.

- *Op Amps for Everyone* (ISBN: 978-0128116487)
- Handbook of Operational Amplifier Applications
- Understanding Basic Analog – Ideal Op Amps
- An Applications Guide for Op Amps

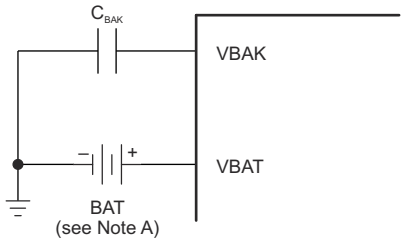
10.2.2.4 Layout Guidelines

Components that are shown in the partial schematic (see Figure 10-8) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal. Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal. When possible, use internal connections to other modules to limit the potential of error introduction.

10.2.3 RTC_B With Battery Backup System

If not using a separate battery backup supply in the system, see Section 7.6 for VBAT and VBAK connections.

10.2.3.1 Partial Schematic



A. BAT can be a battery or super-capacitor. See Section 8.8.8 for specifications.

Figure 10-9. RTC_B With Battery Backup Partial Schematic

10.2.3.2 Retaining an Accurate Real-Time Clock (RTC) Through Main Supply Interrupts

The RTC_B module with Battery Backup System is designed to keep an accurate RTC during main supply interruptions and during low-power modes. For more details on when the Backup Battery System engages, see the Battery Backup System chapter in the MSP430F5xx and MSP430F6xx Family User's Guide. See Using the MSP430 RTC_B Module With Battery Backup Supply for more information and example code on how to keep an accurate RTC through power loss.

10.2.3.3 Charging Super-Capacitors With Built-In Resistive Charger

In applications that use a super-capacitor instead of a battery for secondary supply, the charging circuit functionality of the Battery Backup System can be used to charge the super-capacitor. The resistive charger circuit connects VBAT to DVCC with selectable resistor values found in Section 8.8.8. This means that if DVCC is not present, you cannot use this feature to charge a super-capacitor connected to VBAT. The CTSD16 module can be used to sense the voltage level on VBAT divided by a factor of three. Typical values during VBAT sensing are listed in Section 8.8.8. Channel A8 of the CTSD16 is routed internally for this. See the CTSD16 chapter of the MSP430F5xx and MSP430F6xx Family User's Guide for more information. The BAKADC bit in the BAKCTL register must also be enabled for this feature to operate. Additionally, RTC interrupts can be used to wake up from LPMx.5 states to charge the super-capacitor. While in an LPMx.5 state, the super-capacitor on VBAT drains. This means that the "wakeup to charge" interrupt interval must be designed so that charging starts before the leftover charge in the super-capacitor is too small to accommodate the worst-case backup time if the system were to suddenly lose power. To estimate this time, use Equation 13 for capacitor discharge in an RC circuit.

$$V(t) = V_O e^{\frac{-t}{RC}} \quad (13)$$

Where

- V_O = initial voltage of capacitor
- t = time
- R = circuit resistance
- C = capacitance

Because the operational current is given for when RTC is operating within the specifications section, R can be replaced with $V_O/I_{LPM3.5}$ by Ohm's law. By setting V(t) to the minimum voltage for RTC operation while in backup supply, V_O as voltage of capacitor when fully charged, and C as the super-capacitor capacitance, the estimated RTC operation time can be calculated. If periodic wakeups from LPM3.5 are not desirable for a given application, external means of charging the super-capacitor must be implemented by the user.

For a detailed list of when the secondary supply VBAT powers the backup-supplied subsystem, see the Battery Backup System chapter in the MSP430F5xx and MSP430F6xx Family User's Guide.

10.2.4 LCD_B Peripheral

10.2.4.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, there is flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU which (assuming that the correct choices are made) can be advantageous for the PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However for an example of a schematic using the LCD_B module with an MSP430F6638, see the Ultra Low Power Blood Pressure And Heart Rate Monitor Reference Design.

10.2.4.2 Design Requirements

Due to the flexibility of the LCD_B peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD_B peripheral module chapter in the MSP430F5xx and MSP430F6xx Family User's Guide during the initial design requirements and decision process. The following table provides a brief overview over different choices that can be made and their impact.

OPTION OR FEATURE	IMPACT OR USE CASE
Multiplexed LCD	• Enable displays with more segments • Use fewer device pins • LCD contrast decreases as mux level increases • Power consumption increases with mux level • Requires multiple intermediate bias voltages
Static LCD	• Limited number of segments that can be addressed • Use a relatively large number of device pins • Use the least amount of power • Use only V_{CC} and GND to drive LCD signals
Internal Bias Generation	• Simpler solution – no external circuitry • Independent of V_{LCD} source • Somewhat higher power consumption
External Bias Generation	• Requires external resistor ladder divider • Resistor size depends on display • Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load) • External resistor ladder divider can be stabilized through capacitors to reduce ripple
Internal Charge Pump	• Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications) • Programmable voltage levels allow software-driven contrast control • Requires an external capacitor on the LCDCAP pin • Higher current consumption than simply using V_{CC} for the LCD driver

10.2.4.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_B peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is necessary:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, the segment Sx and common COMx signals are connected to respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_B module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_B module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCDMx register. And consecutive segments are mapped to consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing the most convenient memory layout must be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, refer to the LCD_B controller chapter in the MSP430F5xx and MSP430F6xx Family User's Guide.

For additional design information, see Designing With MSP430 and Segment LCD.

10.2.4.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the V_{SS} pins of the MCU.

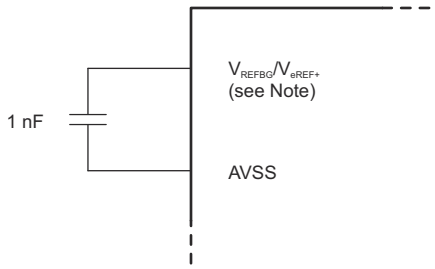
For an example layout of the LCD_B module with an MSP430F6638, see the Ultra Low Power Blood Pressure And Heart Rate Monitor reference design.

10.2.5 DAC12 Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see Section 9.12.16. When available, internal connections should be chosen over external ones to reduce noise and save pins.

Solid decoupling on both the digital and analog supplies is required (best with two capacitors per supply, one 1 µF and one 100 nF [see Section 10.1.1]).

10.2.5.1 Partial Schematic



A. The capacitor is used to reduce noise when using internal VREFBG setting. This pin is also used for the external reference input for the CTSD16 or DAC. When using the external reference, the capacitor is not needed. Because of the shared signal path and pin, the internal and external references (V_{REFBG} and V_{eREF+}, respectively) cannot be used at the same time.

Figure 10-10. DAC12 Partial Schematic

10.2.5.2 Design Requirements

As with any analog signals, appropriate printed-circuit-board layout and grounding techniques must be followed to eliminate ground loops, unwanted parasitic effects, and noise.

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the signal. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

10.2.5.3 Detailed Design Procedure

Digital-to-analog converters (DACs) can be used in a variety of applications and configurations. This section provides some resources for the user to help get started in a design. For details on example DAC applications, see Bridging the Divide: a DAC Applications Tutorial (Precision Signal Path).

Some DAC applications may need an output buffer to reduce the affect of a load on the DAC output. This buffer can be an external op amp or, on some MSP430 devices, the integrated op amp can be used. For more information on how to configure an op amp for this function, see Section 10.2.2.

For more information about DAC applications, see the following application notes:

Digital-to-Analog High-Speed Data Converters Basics

Design for a Wideband Differential Transimpedance DAC Output

10.2.5.4 Layout Guidelines

Application circuits attached to the DAC output should be placed as close as possible to the respective device pins. Avoid long traces because they add additional parasitic capacitance, inductance, and resistance on the signal. Avoid routing analog signals close to a high-frequency pin (for example, a high-frequency PWM) because the high-frequency switching can be coupled into the analog signal. When possible, use internal connections to other modules to limit the potential of error introduction.

10.2.6 USB Module

See the following resources for help with USB design. The application notes contain hardware, software, and application guides and implementations.

Starting a USB Design Using MSP430 MCUs

USB Field Firmware Updates on MSP430 MCUs

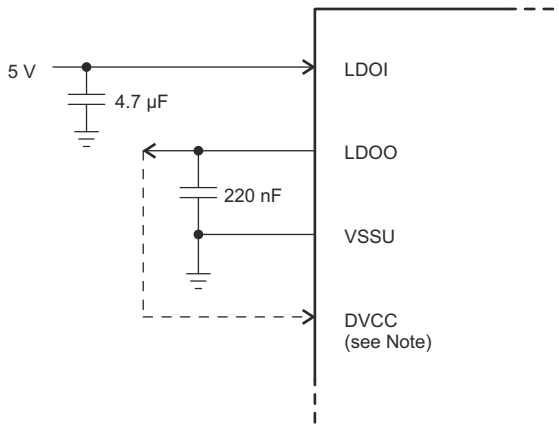
MSP430 USB Developers Package

10.2.7 LDO Module

Solid decoupling on both the digital and analog supplies is required (best with two capacitors per supply, one 1 µF and one 100 nF [see Section 10.1.1]).

The LDO module is in its own power domain on chip (separate from DVCC). To use the Port U pins (PU.0 and PU.1) this domain must be powered. If use of the Port U pins is needed and no voltage is supplied to LDOI, then a 3.3-V supply to LDOO is needed. LDOO can act as an input only when the 3.3-V LDO is not enabled. When the 3.3-V LDO is not needed in applications, keep LDOI tied low to make sure that the LDO module does not draw excessive current when disabled.

10.2.7.1 Partial Schematic



A. Connection between LDOO and DVCC is optional. If connected, the LDO powers the device. LDOO can also supply other subsystems in the application if the maximum output current for the LDO is not exceeded (see the LDO power system specifications in Section 8.8.18.1).

Figure 10-11. LDO Partial Schematic

11 Device and Documentation Support

11.1 Getting Started

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430 ultra-low-power sensing & measurement MCUs overview.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

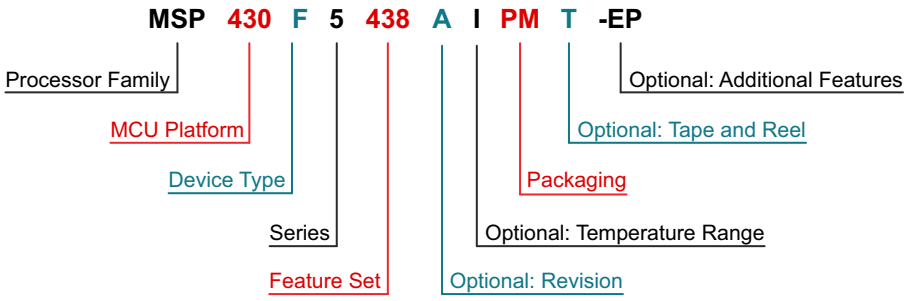
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 11-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory	**Specialized Application** AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series
Feature Set	Various levels of integration within a series	
Optional: Revision	Updated version of the base part number	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified	

Figure 11-1. Device Nomenclature

11.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 ultra-low-power MCUs – Tools & software.

Table 11-1 lists the debug features of the MSP430FG662x and MSP430FG642x MCUs. See the Code Composer Studio IDE for MSP430 MCUs User's Guide for details on the available features.

Table 11-1. Hardware Debug Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT	EnergyTrace++™ TECHNOLOGY
MSP430Xv2	Yes	Yes	8	Yes	Yes	Yes	Yes	No	No

Design Kits and Evaluation Modules

MSP-TS430PZ100AUSB - 100-pin target development board for MSP430FG6x MCUs

The MSP-TS430PZ100AUSB is a stand-alone 100-pin ZIF socket target board used to program and debug the MSP430 MCU in system through the JTAG interface or the Spy-Bi-Wire (2-wire JTAG) protocol.

Educational BoosterPack MKII

The Educational BoosterPack MKII offers a high level of integration for developers to quickly prototype complete solutions. Various analog and digital inputs/outputs are at your disposal including an analog joystick, environmental and motion sensors, RGB LED, microphone, buzzer, color LCD display, and more.

Software

MSP430Ware™ software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of Code Composer Studio™ IDE or as a stand-alone package.

MSP430FG662x, MSP430FG642x code examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP Driver Library

The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

Capacitive Touch Software Library

Free C libraries for enabling capacitive touch capabilities on MSP430 MCUs. The MSP430 MCU version of the library features several capacitive touch implementations including the RO and RC method.

MSP EnergyTrace™ Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC60730 Software Package

The IEC60730 MSP430 software package helps customers comply with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430 MCUs to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 MCUs. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating Point Math Library for MSP430

Continuing to innovate in the low-power and low-cost microcontroller space, TI provides MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating-point math library of scalar functions that are up to 26 times faster than the standard MSP430 math functions. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio integrated development environment (IDE) supports all MSP microcontroller devices. Code Composer Studio IDE comprises a suite of embedded software utilities used to develop and debug embedded applications. Code Composer Studio IDE includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

Uniflash Standalone Flash Tool for TI Microcontrollers

CCS Uniflash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

11.4 Documentation Support

The following documents describe the MSP430FG662x and MSP430FG642x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folders, see Section 11.5). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430FG6626 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430FG6625 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430FG6426 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430FG6425 Device Erratasheet

Describes the known exceptions to the functional specifications.

User's Guides

MSP430F5xx and MSP430F6xx Family User's Guide

Detailed information on the modules and peripherals available in this device family.

MSP430 Flash Device Bootloader (BSL) User's Guide

The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. The document also describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 flash emulation tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller.

Application Reports

Designing With MSP430 MCUs and Segment LCDs

Segment liquid crystal displays (LCDs) are needed to provide information to users in a wide variety of applications from smart meters to electronic shelf labels (ESLs) to medical equipment. This application note helps explain how segmented LCDs work, the different features of the various LCD modules across the MSP430 MCU family, LCD hardware layout tips, guidance on writing efficient and easy-to-use LCD driver software, and an overview of the portfolio of MSP430 devices that include different LCD features to aid in device selection.

MSP430 32-kHz Crystal Oscillators

Selection of the correct crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses different ESD topics to help board designers and OEMs understand and design robust system-level designs.

Using the MSP430 RTC_B Module With Battery Backup Supply

Some applications need to retain an accurate real-time clock (RTC) through battery changes, power outages, and other events. This application note describes how to use RTC_B with battery backup supply functionality to retain the time and keep the RTC counting through loss of main power supply and how to reinitialize when the main power supply is restored.

11.5 Related Links

Table 11-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430FG6626	Click here	Click here	Click here	Click here	Click here
MSP430FG6625	Click here	Click here	Click here	Click here	Click here
MSP430FG6426	Click here	Click here	Click here	Click here	Click here
MSP430FG6425	Click here	Click here	Click here	Click here	Click here

11.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.7 Trademarks

MSP430Ware™, Microstar Junior™, Code Composer Studio™, TI E2E™, MicroStar Junior™, MSP430™, EnergyTrace™, ULP Advisor™, are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export

is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

11.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FG6425IPZR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FG6425	Samples
MSP430FG6426IPZR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FG6426	Samples
MSP430FG6625IPZR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FG6625	Samples
MSP430FG6626IPZ	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FG6626	Samples
MSP430FG6626IPZR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FG6626	Samples
MSP430FG6626IZCAR	ACTIVE	NFBGA	ZCA	113	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG6626	Samples
MSP430FG6626IZCAT	ACTIVE	NFBGA	ZCA	113	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG6626	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

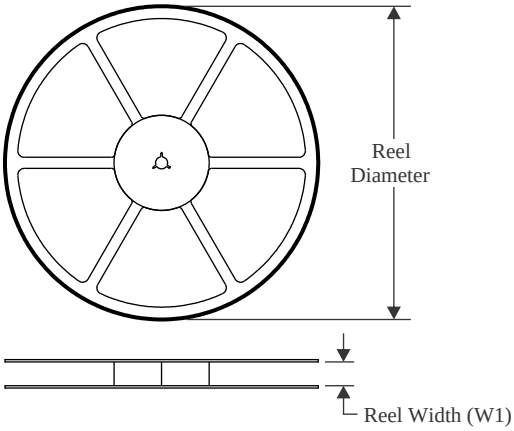
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

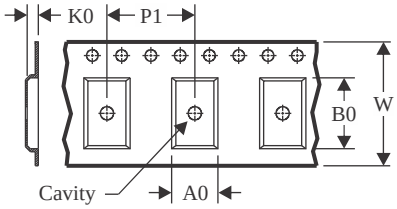
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

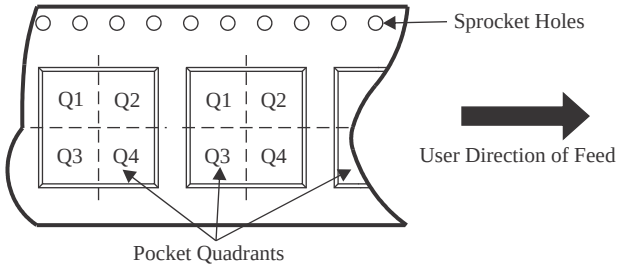


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

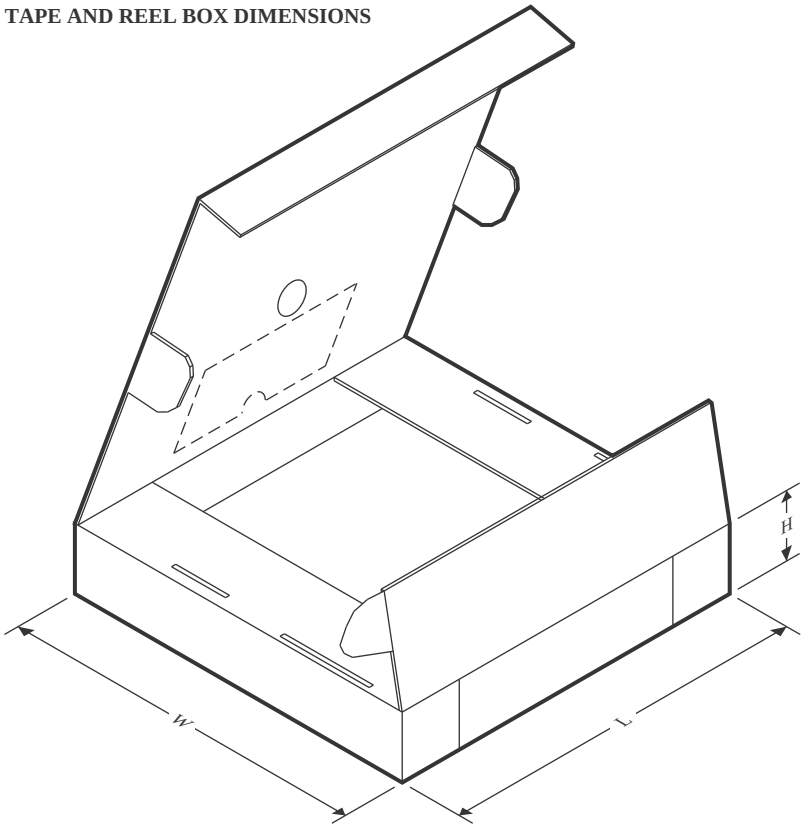
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG6425IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG6426IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG6625IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG6626IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG6626IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

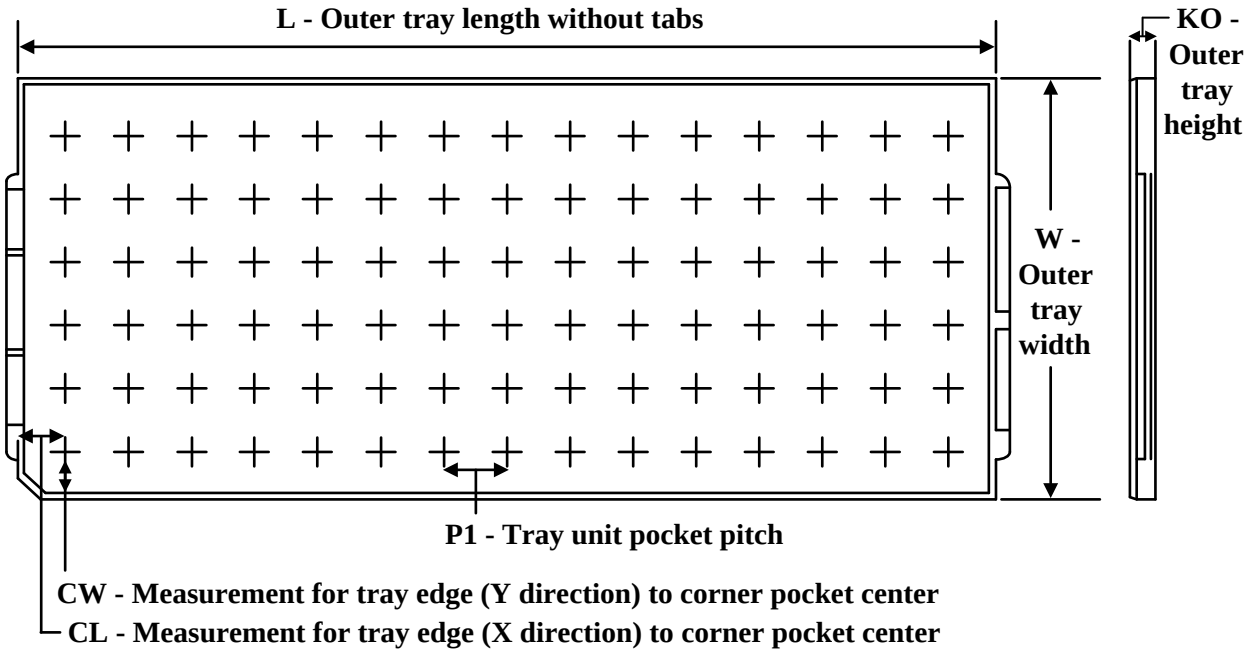
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG6425IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FG6426IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FG6625IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FG6626IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FG6626IZCAR	NFBGA	ZCA	113	2500	336.6	336.6	31.8

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

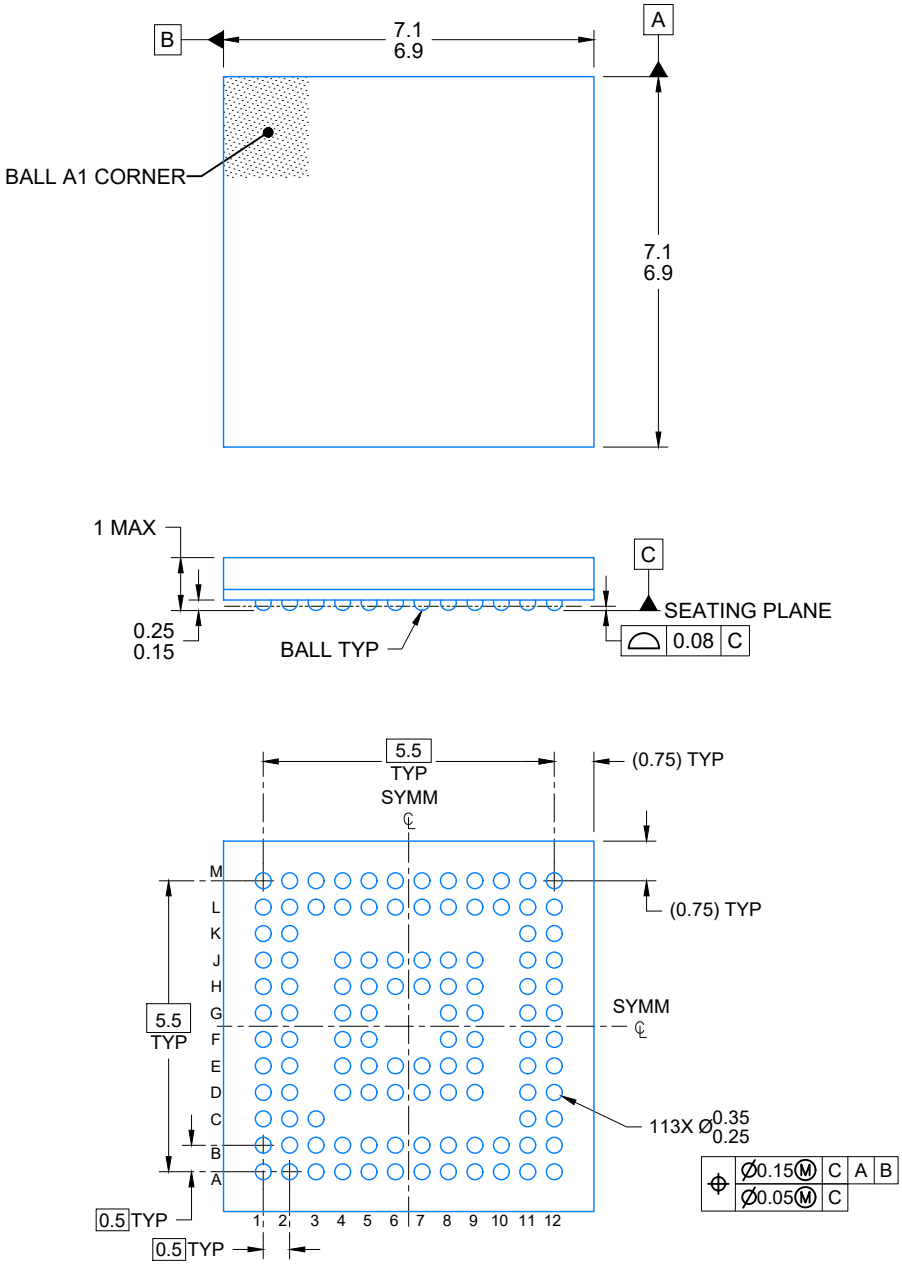
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FG6626IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FG6626IZCAT	ZCA	NFBGA	113	250	10 x 26	150	315	135.9	7620	11.8	10	10.35

PACKAGE OUTLINE

ZCA0113A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



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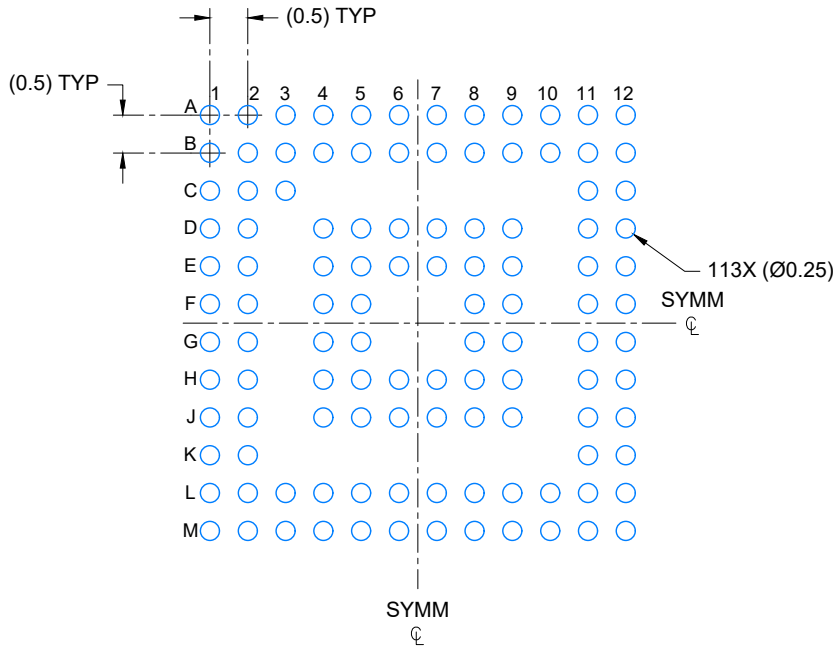
NOTES:

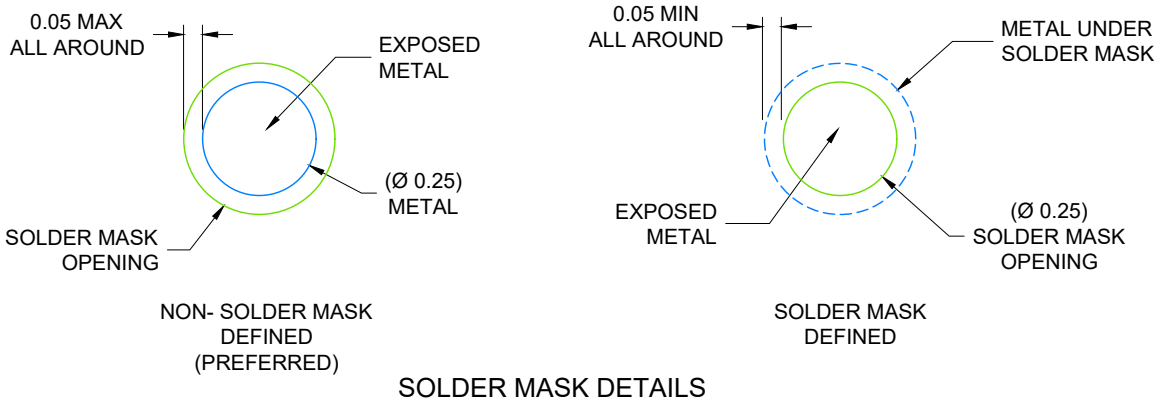
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 10X



SOLDER MASK DETAILS

NOT TO SCALE

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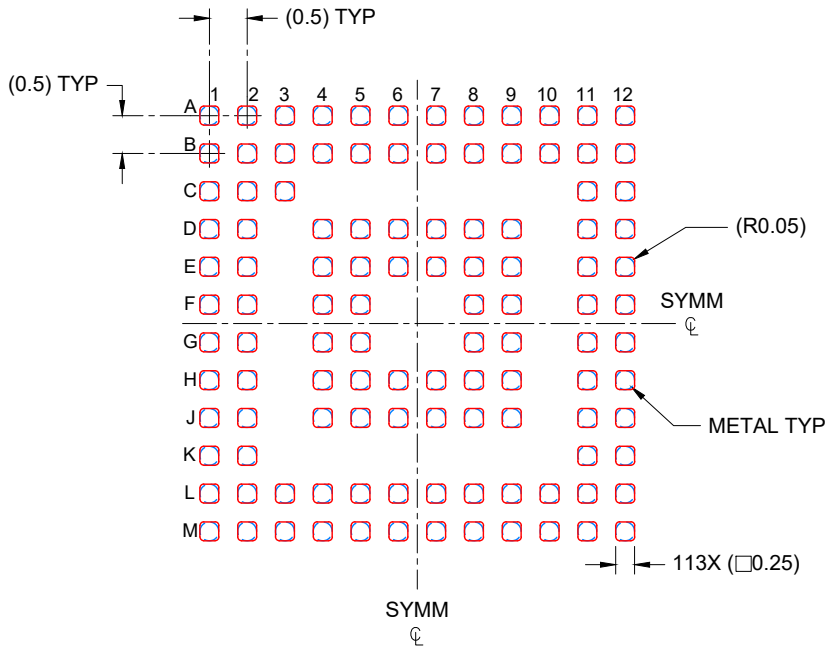
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

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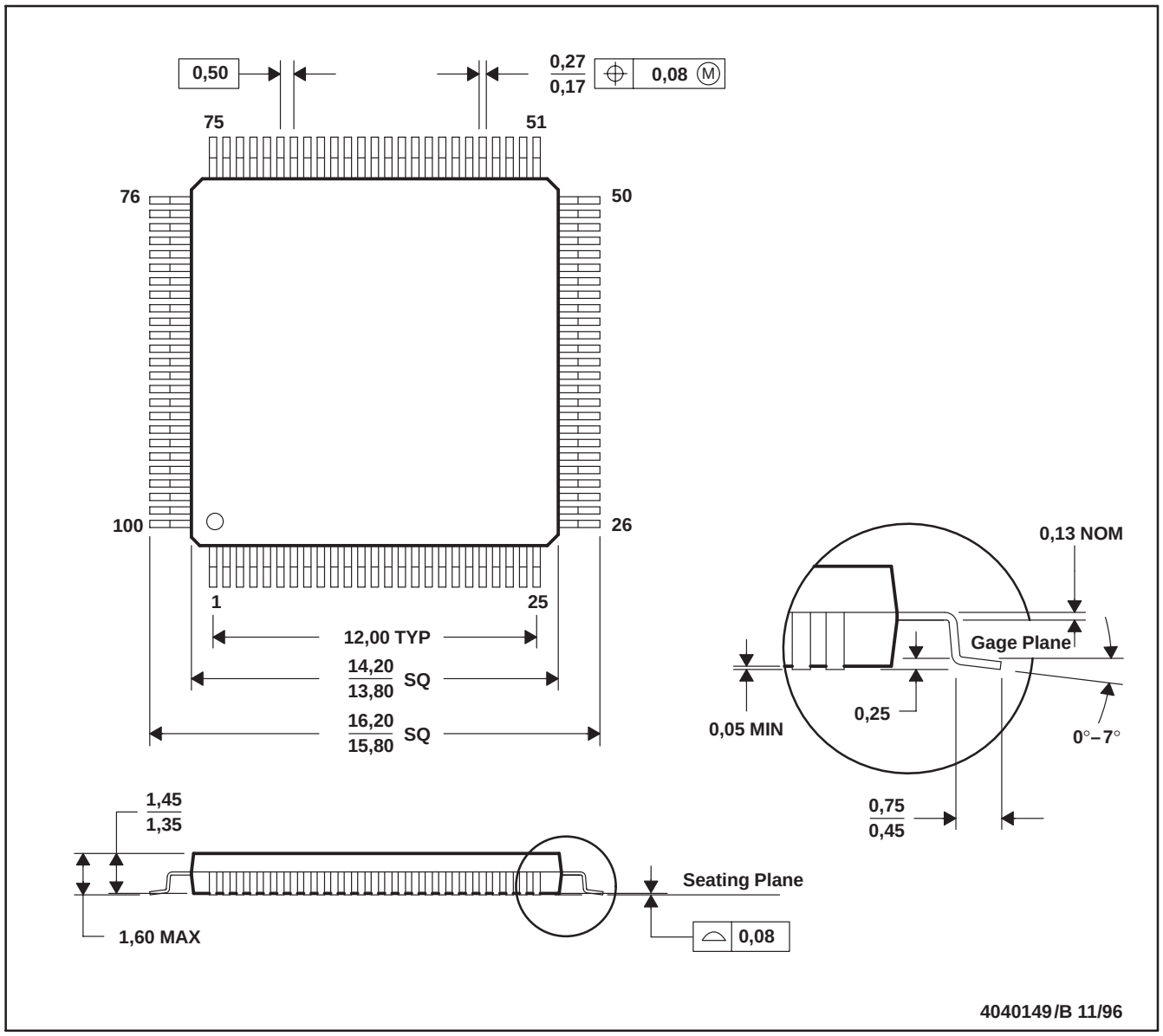
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

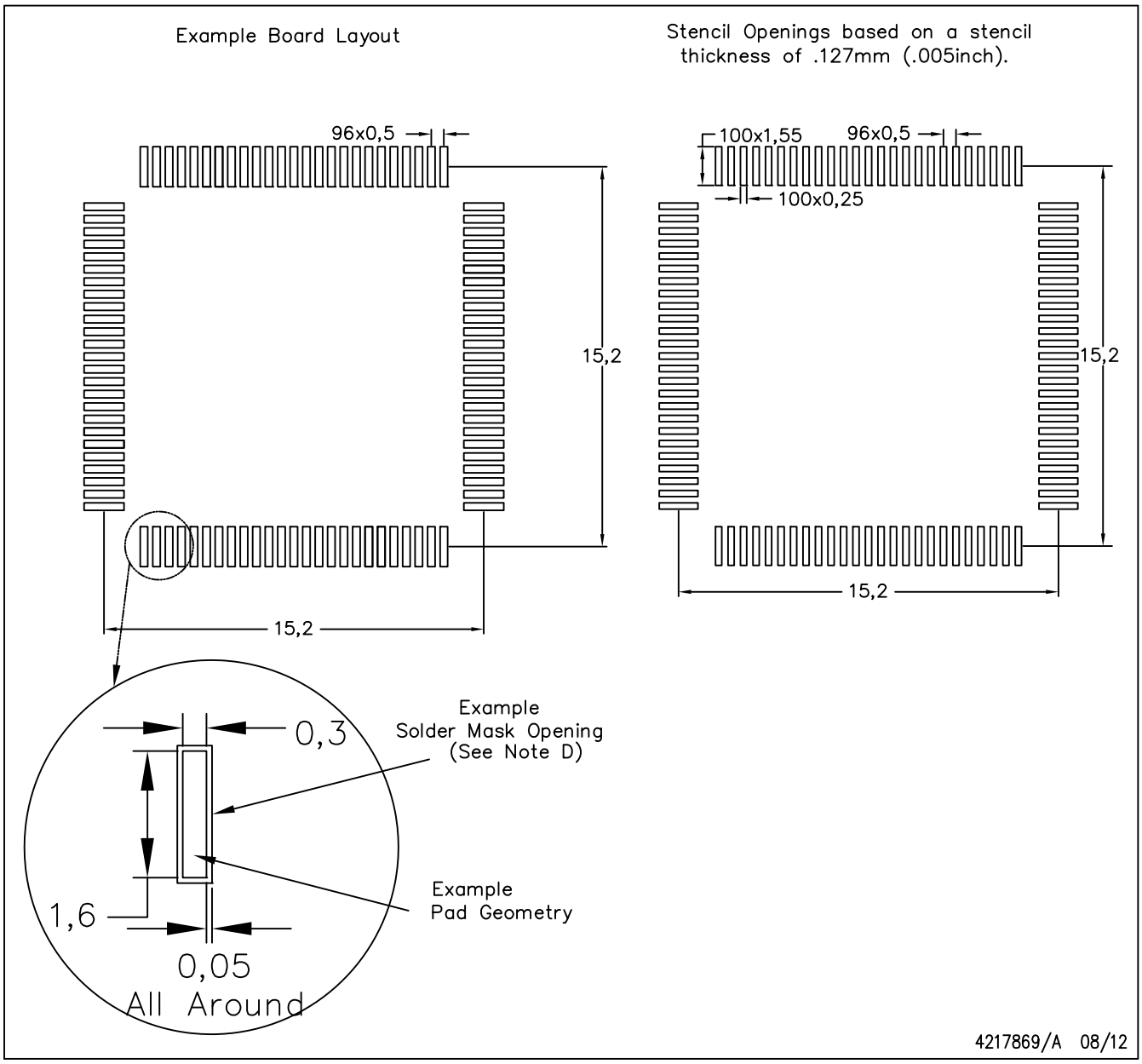
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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