Testing a power supply for line and load transients

Power-supply specifications for line and load transients describe the response of a power supply to abrupt changes in line voltage and load current. By monitoring the supply as it attempts to maintain regulation in the presence of such transients, you can observe any tendency toward output overshoot or oscillation.

Line and load transients are step functions that inject disturbances into the power supply. A load transient injects disturbance into the output by stepping the load current, and a line transient does so by stepping the line voltage. The supply's output response demonstrates its ability to attenuate the various frequency components of a line or load step. The following discussion describes these tests and the information they provide about a power supply.

How are line and load transients generated?

Besides generating artificial disturbances, the test setup for line or load transients must closely reproduce actual operating conditions for the power supply. The test setup must generate steps in line voltage and load current that are fast with respect to the controller's response time, while simulating the supply's operating conditions or end-user specifications. This task requires special attention to layout and component selection. Otherwise, the parasitic inductance, resistance, and capacitance of PC-board traces and components can prevent a fast step response by limiting the required slew rate.

The rise time of the transient should simulate conditions seen by the power supply during operation. If those conditions are not known, the rise time should be fast enough to pull the output out of regulation, thereby eliciting a maximum response from the controller. To do that, the test transient must be faster than the controller's response time. That is, the step transition for a switching converter should occur in less than half a switching period to ensure that the controller is pulled out of regulation.

Knowing the rise time and magnitude of the voltage or current step defines how critical the parasitic inductance, resistance, and capacitance will be in the test setup. For example, consider the need to apply a 10A step with 200ns rise time at the output (V_{OUT} = 1.8V). If the path between output capacitor and load includes 100nH of parasitic inductance, then the fastest possible rise time is 555ns. Parasitic inductance is clearly critical in that case. For a 10A, 10µs step, on the other hand, the parasitic inductance would account for only 5% of the total rise time.

Line transients

Fast line transients can be generated using two n-channel MOSFETs (with low R_{DS_ON}) switching between two DC sources (**Figure 1**). During interval A, Q1 pulls the power-supply input to 5V, while Q2 disconnects the 3V source. During interval B, Q1 disconnects the 5V source and Q2 connects the input to 3V. Note that the drain of Q2 and the source of Q1 both connect to the supply input, thereby preventing unwanted conduction through the MOSFET body diodes.

The gate drive for Q1 and Q2 must rise high enough above the drain-to-source voltage (V_{DS}) to fully turn on the MOSFETs. Though posing a problem for high-voltage inputs, that requirement is easily met for systems of 5V and lower using function generators or MOSFET drivers. The MAX4428 MOSFET driver, for instance, has complementary outputs for driving the two FETs out of phase, and produces a maximum 18V gate drive while sourcing and sinking up to 1.5A. The transient-driver source impedance (composed of R_{DS_ON} for Q1 and Q2, the ESR of C_{BP}, and parasitic inductance) must approximate that of the capacitor (C_{IN}) and its power source, as seen during normal operation by the power supply under test.

Parasitics

Parasitic inductance, resistance, and capacitance in the line transient setup (**Figure 2**) limit the ability of the

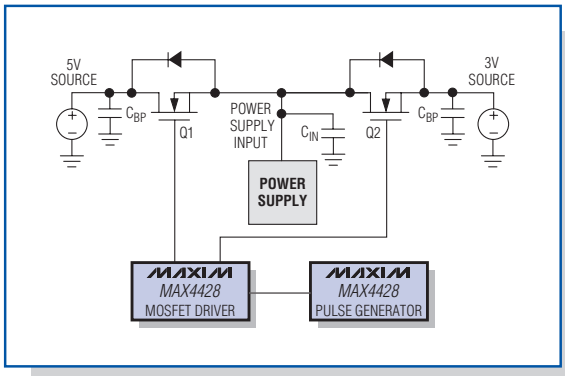

Figure 1. Two n-channel MOSFETs are shown switching between two DC sources, thus generating fast line transients.

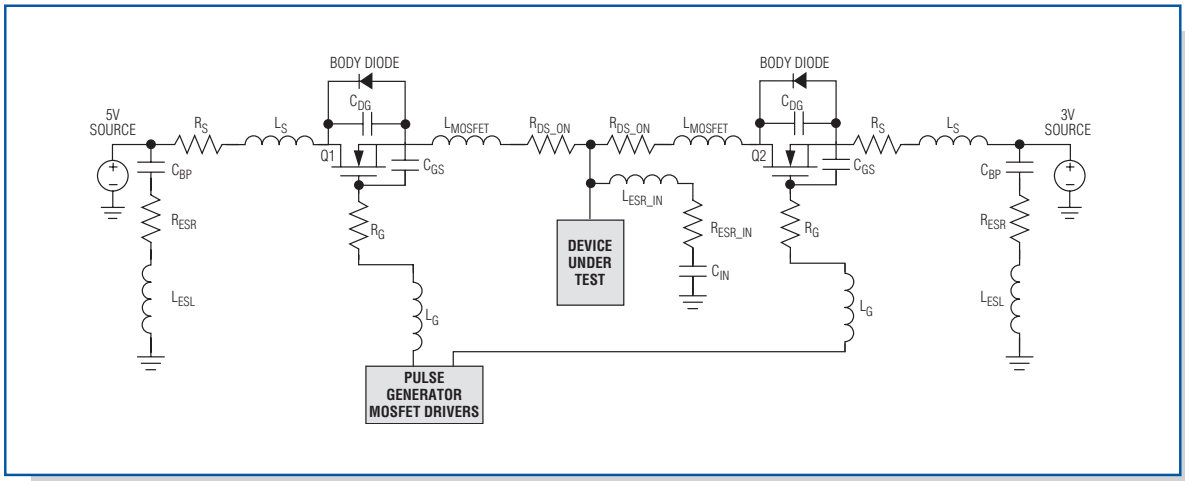

Figure 2. The circuit's ability to deliver a clean step-function waveform is limited by parasitic components in the line-transient setup.

circuit to deliver a clean step-function waveform. To source and sink the large currents necessary, you must minimize series resistance and inductance in the PC board, MOSFETs, and capacitors. Otherwise, the circuit's high capacitance and low series resistance react with the inductance and capacitance at the junction between the MOSFETs and the power-supply input. This produces an underdamped step response (resonance) that causes ringing. The inductance cannot be reduced to zero, but can be reduced to a point where the resonant frequency is high enough to be negligible in comparison with the line transient's rise and fall times.

Source parasitics

Occasionally, the layout requires that C_{IN} must be placed directly at the supply's input. This is because the introduction of a MOSFET between the input bypass capacitor and power-supply input results in unacceptable operation. If this is the case, the line voltage step must be imposed across C_{IN}. To change the voltage by ΔV_{STEP} in time (Δt), the C_{IN} must source or sink a current of

$$I = C_{IN} \times \frac{\Delta V_{STEP}}{\Delta t}$$

The bypass capacitors (C_{BP}) must be low-R_{ESR} ceramics with value much larger than C_{IN}. That condition minimizes the voltage drop across R_{ESR} at the currents necessary to charge and discharge C_{IN} in the time required.

Even with ceramic bypass capacitors, the series inductance of the capacitor (L_{ESL}) and of the connections between C_{IN} and C_{BP} (L_S) can pose a restriction on fast rise times and large currents. A few nanohenries of inductance can limit the current rise time (t) required to produce a reasonable voltage step at C_{IN}. For example, if C_{IN} = 100µF and ΔV = 1V, the circuit must source 100A into C_{IN} to step the voltage in 1µs. If the connection between C_{BP} and C_{IN} includes 100nH of parasitic inductance, the time required to raise the C_{IN} voltage by 1V is 2µs. Too much parasitic inductance can also cause excessive overshoot or ringing, which prevents the line transient from being a clean step function.

Parasitic resistance and inductance can be reduced by connecting smaller-valued ceramic capacitors in parallel. That arrangement reduces the total equivalent impedance by paralleling the R_{ESR} and L_{ESL} of the multiple capacitors. You can also reduce the inductance by using leadless capacitors or multilayer ceramic chip capacitors (MLCCs), or both. The distance from the bypass capacitors to the drains of the MOSFETs can also add impedance. PC-board traces of 2mm-wide, 1oz copper contribute parasitics of about 25mΩ/cm and 5nH/cm. You can minimize this additional impedance by making the connections between the bypass capacitors and MOSFET drains as wide and short as possible.

MOSFET parasitics

The parameters driving the selection of MOSFETs Q1 and Q2 are primarily the on-resistance (R_{DS_ON}), package size, and gate capacitance. R_{DS_ON} is important for the same reasons as the PC-board resistance and R_{ESR} of the bypass capacitors. Higher resistance limits current into the input capacitance (C_{IN}), and also causes excessive voltage ripple due to the pulsed currents of switching power supplies. Low R_{DS_ON} is especially important, because

R_{DS_ON} is the primary source of resistance in the capacitors' charge/discharge path.

The MOSFET series inductance, which includes the drain-to-source inductance and the inductance of the internal bond wires and leads, adds impedance in series with the power sources. Smaller MOSFET packages have less inductance because the bond wires and lead lengths are shorter. Identical MOSFET chips in D^2PAK and 8-pin SO packages, for example, show total series inductances of 10nH and 3.2nH respectively.

MOSFETs with very low on-resistance normally have higher gate capacitance (C_{GS}), which generally requires the use of MOSFET drivers capable of quickly charging and discharging C_{GS}. Drivers like the MAX4428 are useful because they can quickly turn on MOSFETs with several nanofarads of gate capacitance. To reduce the inductance and resistance that slow the rise time of the gate voltage, keep the trace lengths between driver and MOSFET gate short and wide.

When you have minimized the inductance and resistance of the capacitors' charge/discharge paths, the MOSFETs can be connected—either between the power-source bypass capacitors and the power supply's input capacitor or, if possible, directly to the supply input. In the latter case, the power-source bypass capacitors serve as input capacitance for the power supply. In either case, make the connection from the MOSFETs to C_{IN} or from the MOSFETs to the power-supply input as short as possible to minimize parasitic inductance and resistance contributed by the PC board.

Load transients

A good method for generating load-transient steps is to use an n-channel MOSFET to switch between two different load resistances at the power-supply output. For transient tests with large output currents, the MOSFET itself can be the load element (**Figure 3**). The MOSFET drain in that configuration connects to the power-supply output, and its source connects to ground through a current-sense resistor. The load resistance is adjusted by stepping the gate-to-source voltage (V_{GS}). As long as the MOSFET operates outside its saturation region, adjusting V_{GS} will vary the MOSFET R_{DS_ON}, and thus the load current.

To avoid adding extra inductance in the current-measuring loop, you should use a low-inductance current-sense resistor. Too much inductance limits the rise time of the output-current step, and causes ringing between the drain-to-source capacitance (C_{DS}) and the parasitic trace inductance (L_{PARA}), as illustrated in Figure 3. In this configuration, the sense resistor is part of the load.

The MOSFET must be placed directly across the output capacitor (C_{OUT}). Smaller MOSFET packages or MOSFETs in parallel can further reduce the L_{PARA}. To allow fast and clean switching, the connection between MOSFET gate and pulse generator (or MOSFET driver) must be short and wide to minimize trace inductance and resistance (R_G and L_G).

For smaller loads ($R_{LOAD} >> R_{DS\_ON}$), connect the MOSFET between ground and the load resistor R_A (bold lines of Figure 3). Connect another load resistor (R_B) in parallel with the MOSFET. When the MOSFET is on, the load resistance is R_A; when it is off, the load resistance is $R_A + R_B$. For the latter setup, pay close attention to the added inductance of the resistors and leads (L_R) that connect the load to the power supply's output capacitors. You can minimize that inductance by making the connections to R_A and R_B as short as possible. Avoid wire-wound resistors because they add excessive inductance. Power metal-film resistors are preferred.

What do line and load transients tell us about a power supply?

Having explained how line and load transients are generated, we now ask what information do they give about a power supply? As background, we must first understand the action of feedback and the effect of

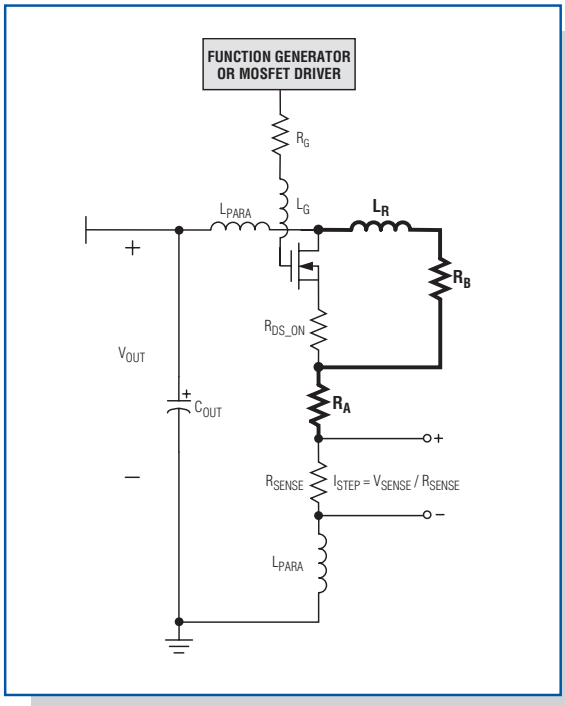

Figure 3. The MOSFET can be the load element in a load-transient test with parasitics labeled.

frequency response on the power-supply control loop and its response to line and load transients.

Loop gain attenuation

First, the effects of feedback on the small-signal gain of the power-supply controller must be understood. A simplified diagram for a buck converter with no feedback is shown in **Figure 4a**. Line and load steps are represented as inputs $I_{LOAD}(s)$ and $V_{IN}(s)$. The effect at the output from line and load disturbances is:

$$V_{OUT}(s) = V_{IN}(s) \times G_{VIN}(s) - I_{LOAD}(s) \times Z_{OUT}(s)$$

where $Z_{OUT}(s)$ is the output impedance.

The controller's power-filter gain ($G_{VIN}(s)$) is the small-signal gain from input to output. The buck converter, for example, has a power-filter gain of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{D}{s^2 LC_{OUT} + s\frac{L}{R_{LOAD}} + 1} = G_{VIN}(s)$$

where D is the controller's duty cycle. L, C_{OUT}, and R_{LOAD} are shown in **Figure 4b**.

Output impedance for the buck converter is:

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = R_{LOAD} \left\| \frac{1}{sC_{OUT}} \right\| sL = \frac{sL}{s^2 LC_{OUT} + \frac{sL}{R_{LOAD}} + 1}$$

where R_{LOAD} is the controller's DC operating load.

With no feedback, any disturbance of input voltage or load current propagates through and affects the output voltage directly. For example, the buck converter operating with V_{IN} = 12V and a 50% duty cycle has a 6V output voltage. A 2V step in the input voltage, therefore, produces a 1V change in the output voltage. With the introduction of feedback, the output is made to regulate to a set reference (V_{REF}), shown by the bold lines in Figure 4a. The gain from line and load disturbances is now:

$$V_{OUT}(s) = \frac{V_{REF}(s) \times G_C(s)}{1 + G_{FB} \times G_C(s)} + \frac{V_{IN}(s) \times G_{VIN}(s)}{1 + G_{FB} \times G_C(s)} - \frac{Z_{OUT}(s) \times I_{LOAD}(s)}{1 + G_{FB} \times G_C(s)}$$

The above equation describes the closed-loop gain. The addition of feedback reduces line voltage and load current disturbances by the factor $(1 + G_{FB} \times G_C(s))$, where G_{FB} is the feedback-divider gain and $G_C(s)$ is the controller gain. The controller gain includes the gain for the power filter, the error amplifier, and other gain elements in the control loop. The term $G_{FB} \times G_C(s)$ is the open-loop gain. A Bode plot of open-loop gain shows the effect of feedback on the attenuation of V_{IN} and I_{LOAD} disturbances, with respect to frequency. Of special interest is the crossover frequency (f_C), at which $|G_{FB} \times G_C(s)| = 1$, and its associated phase shift (the phase margin). Phase margin is the difference between 180° and the phase shift at f_C. As the margin approaches 0°, the system exhibits unwanted effects at frequencies near f_C.

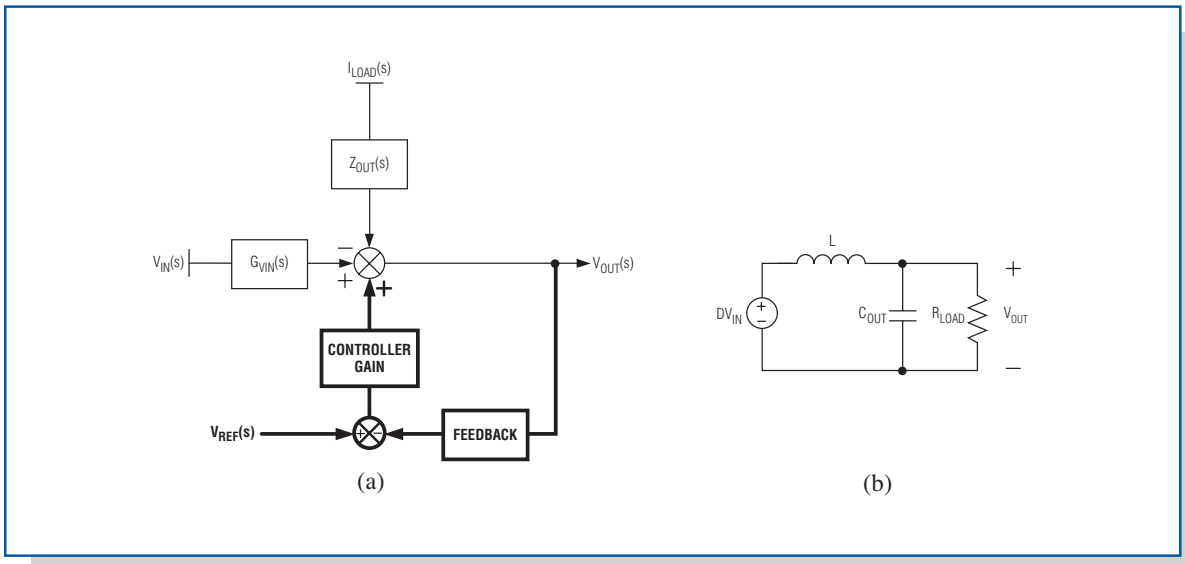

Figure 4. A simplified diagram and schematic for a buck converter is illustrated without feedback (a) and with feedback (b).

The frequency response is related to the transient response, because line and load transients are step functions, composed of an infinite sum of frequencies with amplitudes proportional to $1/f$. A step function is normally written in its frequency domain representation as 1/s, where s is the complex quantity jω.

Time domain to frequency domain

The transient response of a power supply with single-pole open-loop gain is a good example of what happens during a line or load transient. If the open-loop gain has only a single pole, it can be expressed as:

$$G_{FB} \times G_C(s) = \frac{DC_{GAIN}}{\left(\frac{s}{\omega_0} + 1\right)}$$

where DC_{GAIN} is the open-loop DC gain. **Figure 5a** shows a single-pole Bode plot in which the gain rolls off at -20dB/decade and crosses unity with 90° of phase margin. As the open-loop gain decreases with frequency, so does the attenuation of higher-frequency disturbances from V_{IN} and I_{LOAD}. By multiplying the closed-loop gain

$$\left(\frac{1}{(1 + G_{FB} \times G_C(s))}\right)$$

by the frequency-domain step function 1/s, and taking the inverse Laplace transform, you obtain the time-domain response to a step function (**Figure 5b**). A load step (ΔI_{LOAD}) applied to a controller with this open-loop gain exhibits an exponential response in the time domain, with an initial drop in the output equal to $\Delta V = I_{LOAD}(s) \times Z_{OUT}(s)$. At higher frequencies, $Z_{OUT}(s)$ is dominated by the capacitor impedance, which consists of the series resistance (R_{ESR}) and series inductance (L_{ESL}). Recovery takes the form:

$$V(t) = \frac{\Delta V}{1 + DC_{GAIN}} \times \left(1 + DC_{GAIN} \times e^{-(\omega_0 + \omega_0 DC_{GAIN})t}\right)$$

At one time constant ($\tau \approx 1/2\pi f_C$), the output voltage has recovered 63% of the initial drop (ΔV). Similarly, a line step raises the voltage at the output by the $G_{VIN}(s)$ multiplied by $V_{IN}(s)$. After one time constant ($1/2\pi f_C$ again), the output voltage has recovered 63% of the initial excursion.

An open-loop gain expression normally exhibits multiple poles, which results in a phase margin of less than 90°. If the phase margin of the open-loop gain is allowed to approach 0°, the closed-loop system response to a transient begins to show overshoot, and eventually oscillation. These output disturbances, which warn of the possibility of marginal stability or instability in the power-supply control loop, are the indicators to monitor when performing a transient test.

The closed-loop response shows overshoot and oscillation when it goes from attenuating frequency components of the transient to providing gain to them. That action is explained by interactions between the real and complex quantities in the denominator of the closed-loop gain. As the open-loop phase margin approaches 0°, its real portion

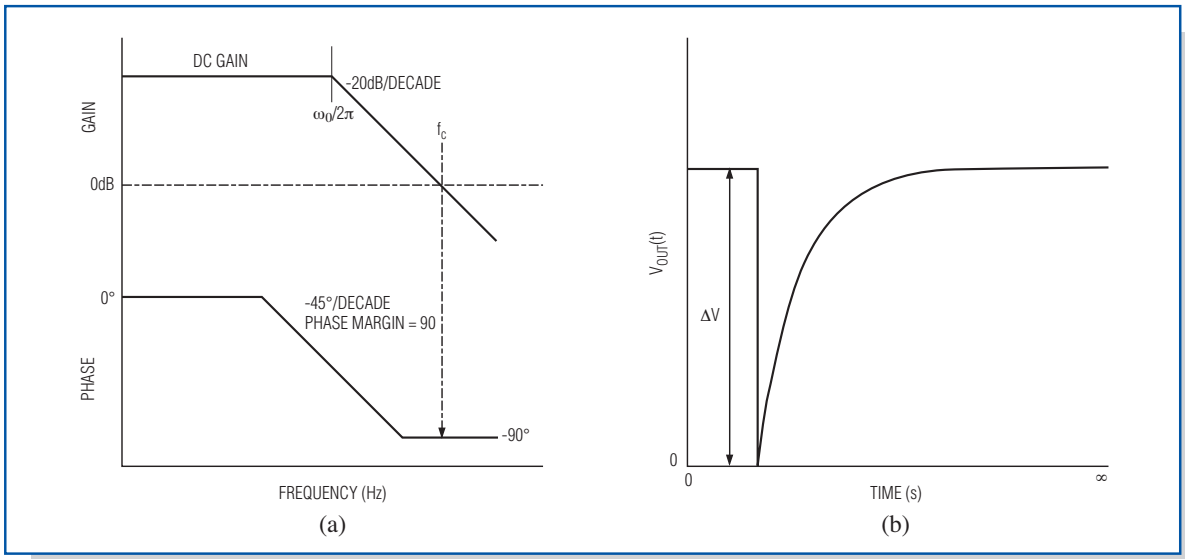

Figure 5. The Bode plot of single-pole loop gain is shown (a), as well as the time-domain response to a step function (b).

approaches -1 and its imaginary portion becomes less than 1. Also, the magnitude of the open-loop gain approaches unity. In the denominator of the closed-loop gain, the real parts sum to zero, leaving only the small imaginary portion. As a result, the closed-loop system that normally attenuates signals now provides gain to them.

A two-pole, open-loop gain expression gives a good example of what happens to a step response as you decrease the phase margin. Consider an open-loop gain with DC_{GAIN} = 60dB, designed with two real poles:

$$G_{FB} \times G_C(s) = \frac{1000}{\left(\frac{s}{\omega_1} + 1\right)\left(\frac{s}{\omega_2} + 1\right)}$$

The closed-loop gain is:

$$\frac{1}{1 + G_{FB} \times G_C(s)}$$

Assume that f_C occurs between ω1 and ω2. You then vary ω1 and ω2 to change the phase margin while maintaining f_C constant. Each separate phase margin has a separate step response in the time domain. By running the step() command in MATLAB®, you can obtain the time-domain response of the closed-loop gain with a two-pole, open-loop gain for various phase margins (**Figure 6**).

Figure 6 shows several transient responses possible at the output of a power supply with different phase margins. The initial step raises the output voltage. As the supply comes back into regulation with decreasing phase margin, the output shows increasing overshoot and eventually full oscillation. The fastest recovery with 0% overshoot occurs for a phase margin near 72°.

Load transient, practical example

Figures 7a/b/c show a 0 to 10A load transient with a buck converter using voltage mode control (see MAX1960EVKIT at www.maxim-ic.com). After adding a high-frequency pole at the COMP pin to reduce the gain above crossover, the open-loop gain and phase are measured at V_{IN} = 5V, V_{OUT} = 1.8V, and I_{LOAD} = 10A. Reducing the frequency of this pole decreases the phase margin. Figure 7a shows the response with an open-loop crossover frequency of 42kHz and 2° of phase margin. A load step from 0 to 10A causes the power supply to go into continuous oscillation. Increasing the phase margin to 11° damps the oscillation (Figure 7b). With 90° of phase margin (Figure 7c), the output response is that of an exponential single pole.

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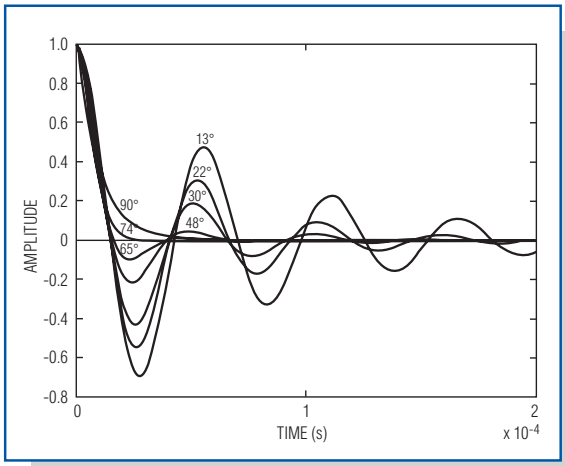

Figure 6. MATLAB step( ) commands can be run to obtain a time-domain response for closed-loop gain with various phase margins.

The small-signal frequency response for this circuit predicted that, with 2° of phase margin, the power-supply output would oscillate. Why does it not oscillate when the load steps back to 0A? The conditions at 0A do not support oscillation, because the small-signal response changes with the operating condition (bias point). The initial phase margin was measured at I_{LOAD} = 10A, V_{IN} = 5V, and V_{OUT} = 1.8V. When any of those parameters change, the small-signal gain and phase margin also change. This effect is seen in the 10A to 0 load step. When I_{LOAD} steps to 0A, the oscillation becomes damped. This is because the phase margin improves when operating with a 0A load (as opposed to a 10A load).

Be careful when attempting to equate the small-signal response predicted by open- and closed-loop transfer functions to large-signal changes like line and load transients. The small-signal responses are valid only for small changes around a specific operating point. Large-signal changes alter the bias point, which in turn changes the open-loop gain and phase. Only transients that occur at the specific operating point can be predicted by the small-signal response.

The load transient was generated using a single n-channel MOSFET (IRLR024N) in a DPAK package. The MOSFET was placed directly on top of one of the output capacitors, with a 37.5mΩ low-inductance sense resistor between the source and ground. A pulse generator (HP8112) directly stepped the gate from 0 to 4V, generating step responses from 0 to 10A in 200ns with virtually no overshoot or ringing.

Line transient, practical example

Figure 7d shows the line-transient response, with the same phase margin as in Figure 7c. The input voltage is stepped from 3.3V to 5V. Using the setup from Figure 1, two 9mΩ, n-channel MOSFETs (IRF3704, TO-220 package) switch the input of the supply under test between a 3.3V source and a 5V source. Each switch was placed between the MAX1960 input and two 470µF POSCAPs (6TPB470M) in parallel. Rise times of 400ns with 250mV overshoot were developed to simulate the line step.

Small-signal Bode plots predicted that the response should be exponential, which was verified. Stepping V_{IN} from 3.3V to 5V is a large-signal swing, and thus a different operating point is obtained when the power supply operates at V_{IN} = 3.3V. This transient test indicates that, at either input voltage, the phase margin is sufficient to prevent overshoot or ringing.

A similar article appeared in the July, 2004 issue of Power Electronics Technology.

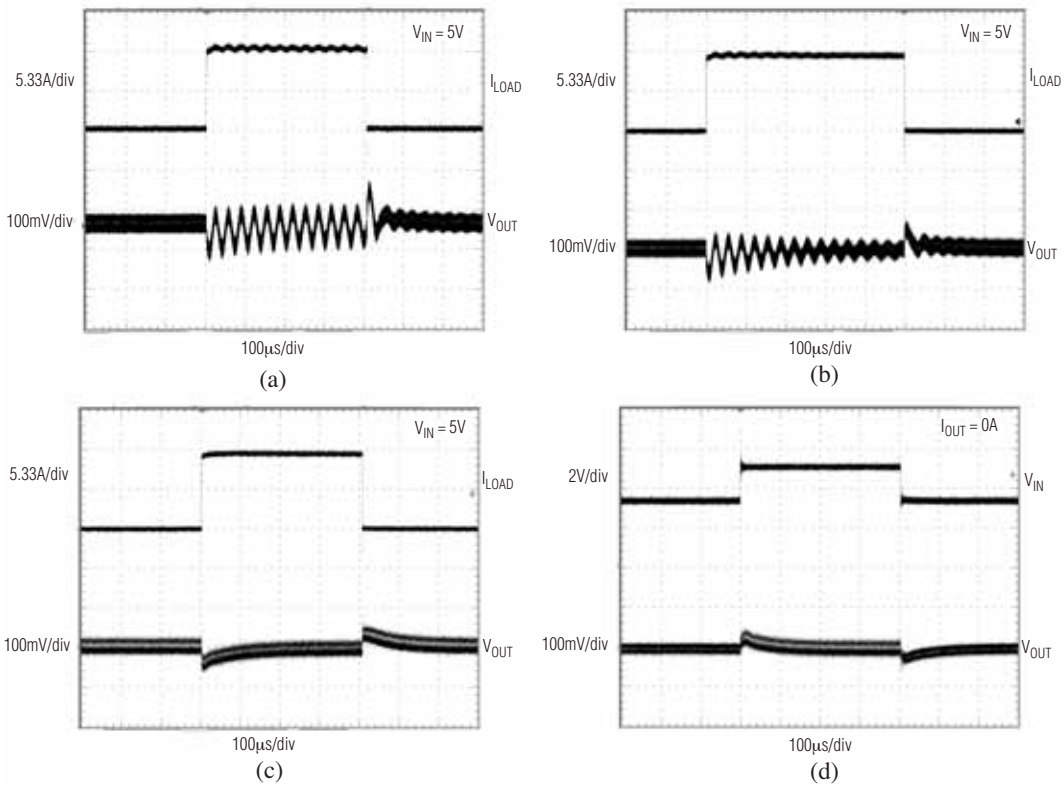

Figure 7. EV kit transient responses are shown for: a load step with 2° phase margin (a); a load step with 11° phase margin (b); a load step with 90° phase margin (c); and a line step with 90° phase margin (d).