

U_FPGA_PWR_MISC
FPGA_PWR_MISC.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

U_B14_B16
B14_B16.SchDoc

U_B15
B15.SchDoc

U_B34
B34.SchDoc

U_B35
B35.SchDoc

U_SystemController
SystemController.SchDoc

U_FTDI
FTDI.SchDoc

U_POWER
POWER.SchDoc

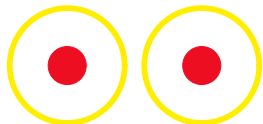
U_B2B_Connector
B2B_Connector.SchDoc

LOGO1

TE Logo PRINT Layer

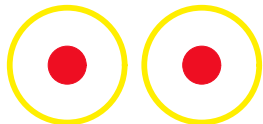
LOGO PRINT

Top of Board



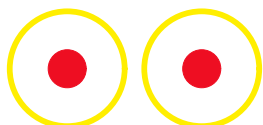
PM1

PM2



PM4

PM5



PM6

PM3



Screw M3x4

Distance Holder M3x8

Screw M3x6

Screw M3x4

Distance Holder M3x8

Screw M3x6

Screw M3x4

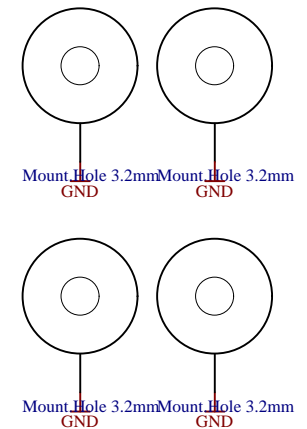
Distance Holder M3x8


Screw M3x6

Screw M3x4

Distance Holder M3x8

Screw M3x6



			Title: TE0711	
			A4	Number: TE0711 TE0711-35-2C
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1

2

3

4

A

A

B

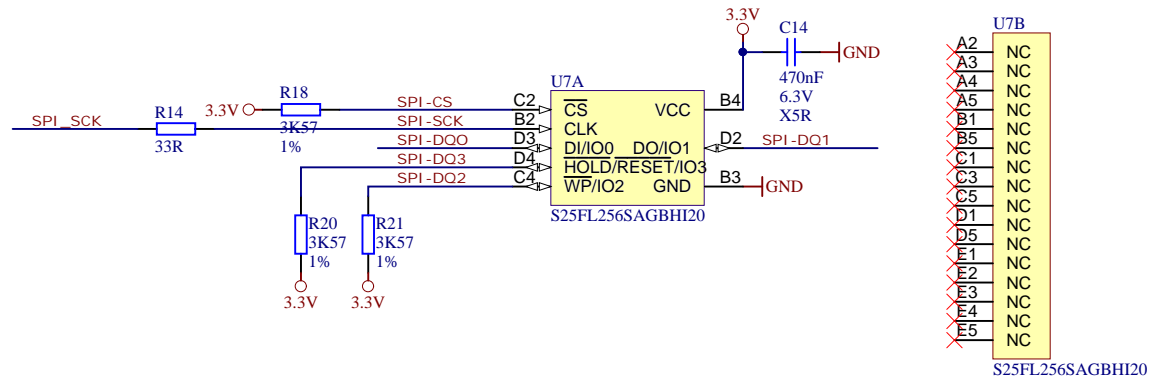
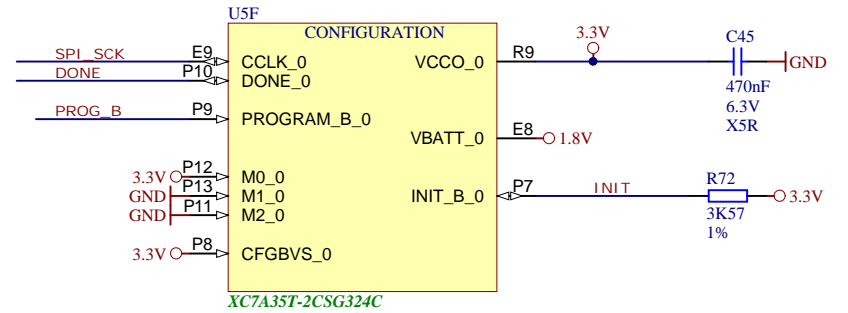
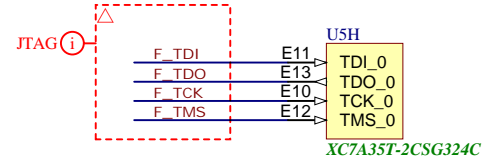
B

C

C

D

D



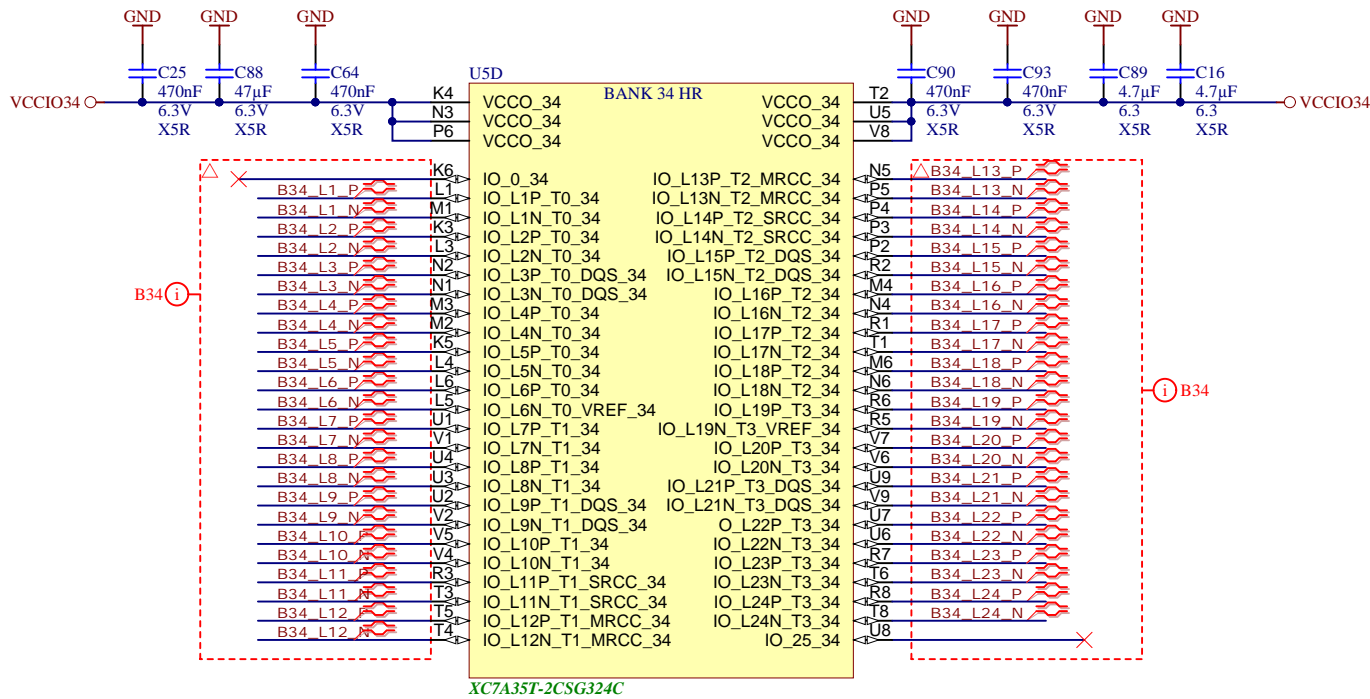
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	A4	Number: TE0711 TE0711-35-2C
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Filename: FPGA_CFG.SchDoc		Rev. 01

1

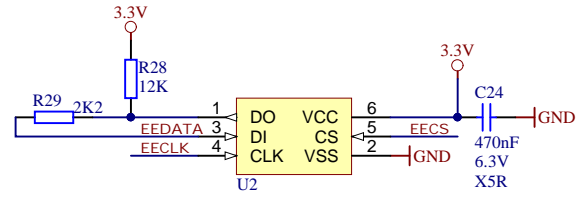
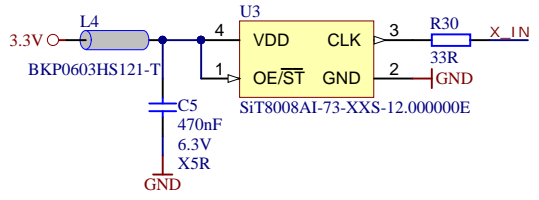
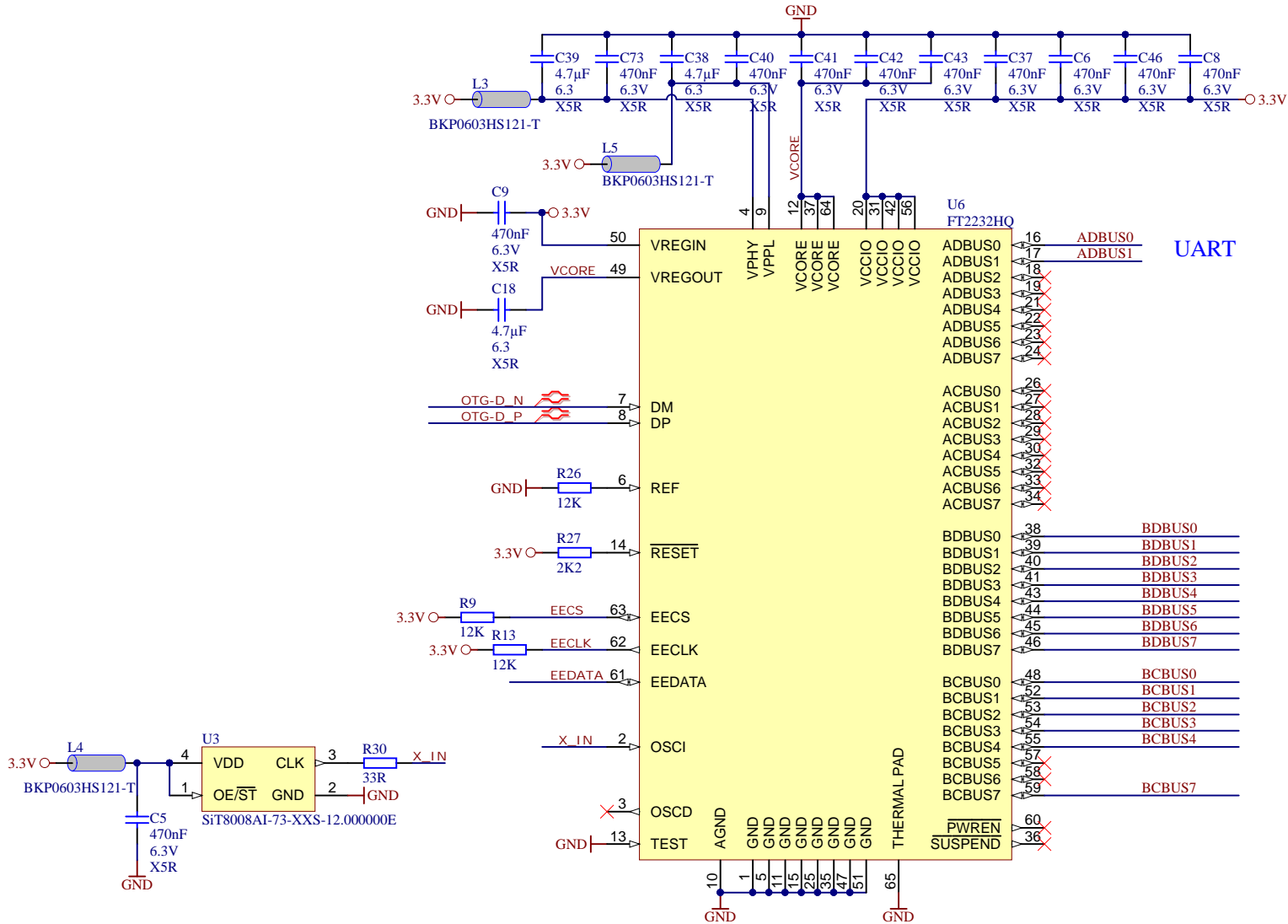
2

3

4



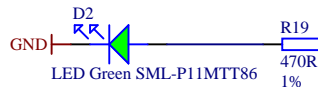
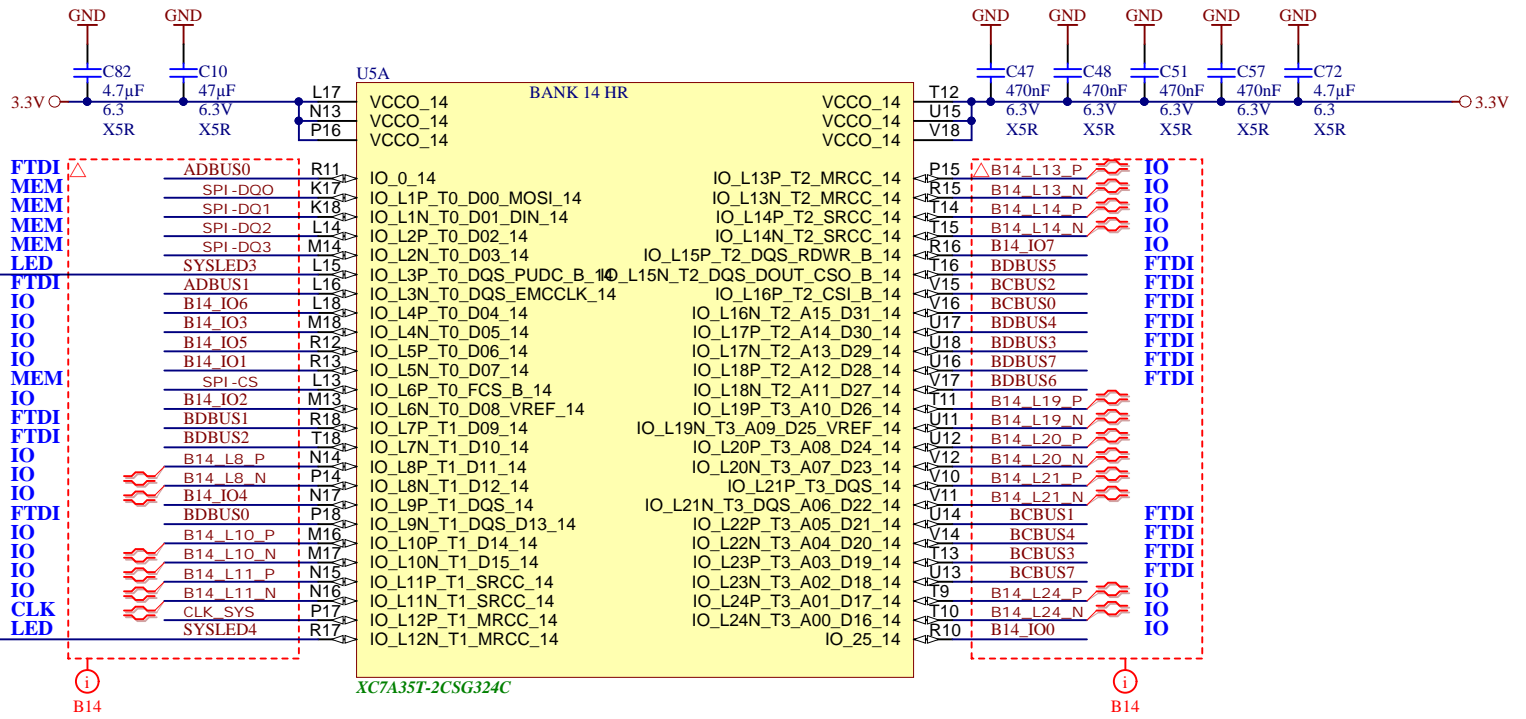
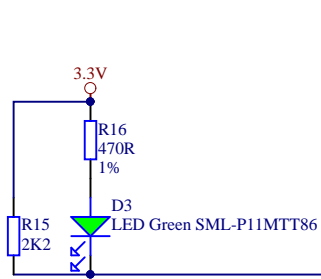
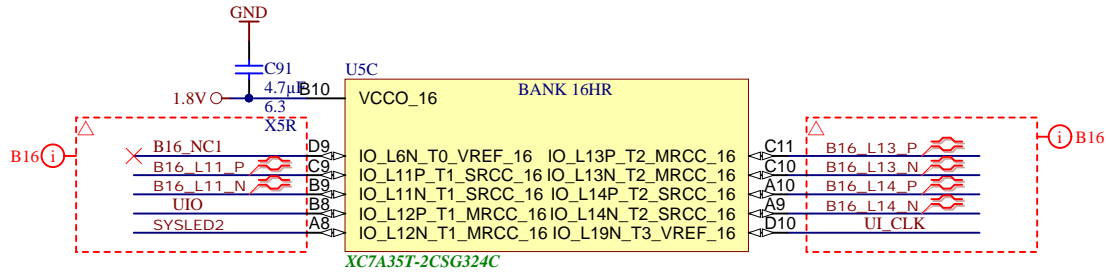
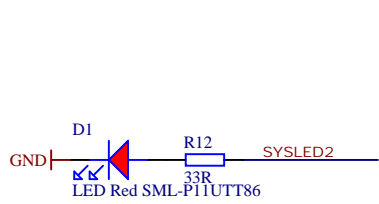
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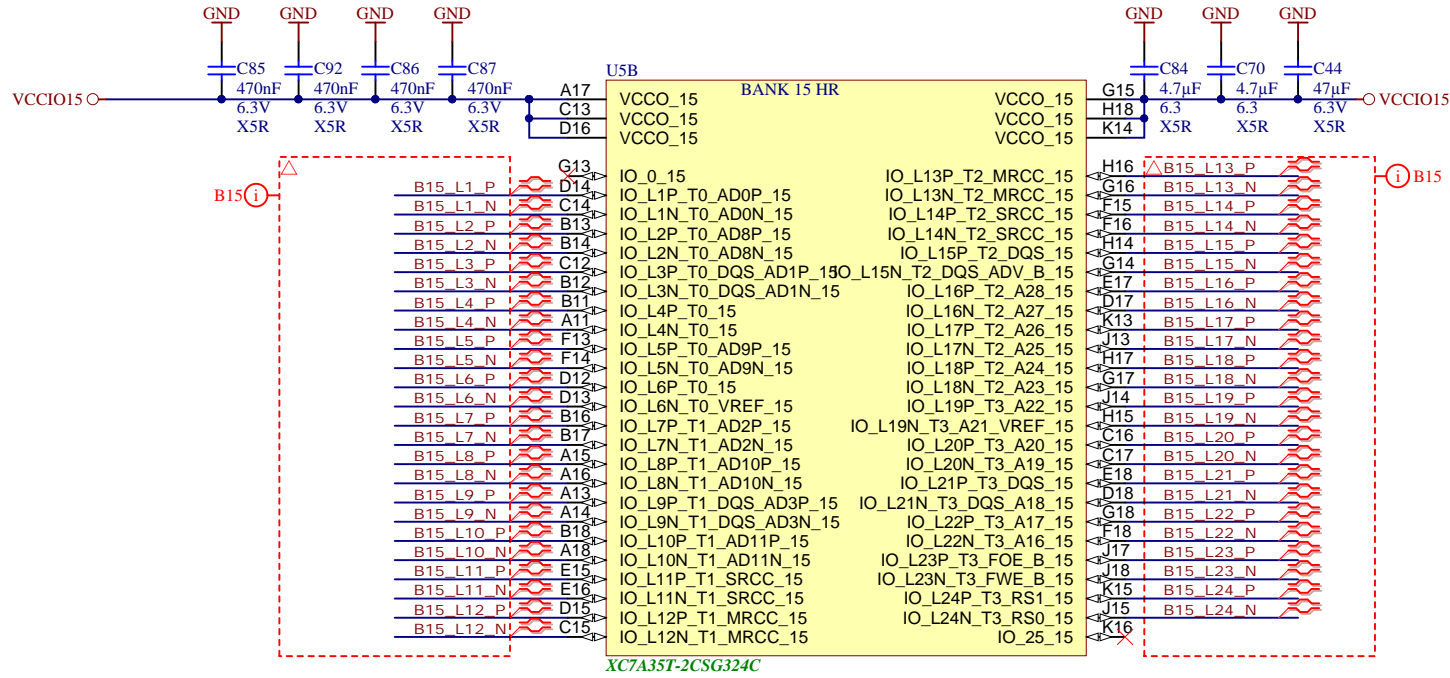

UART



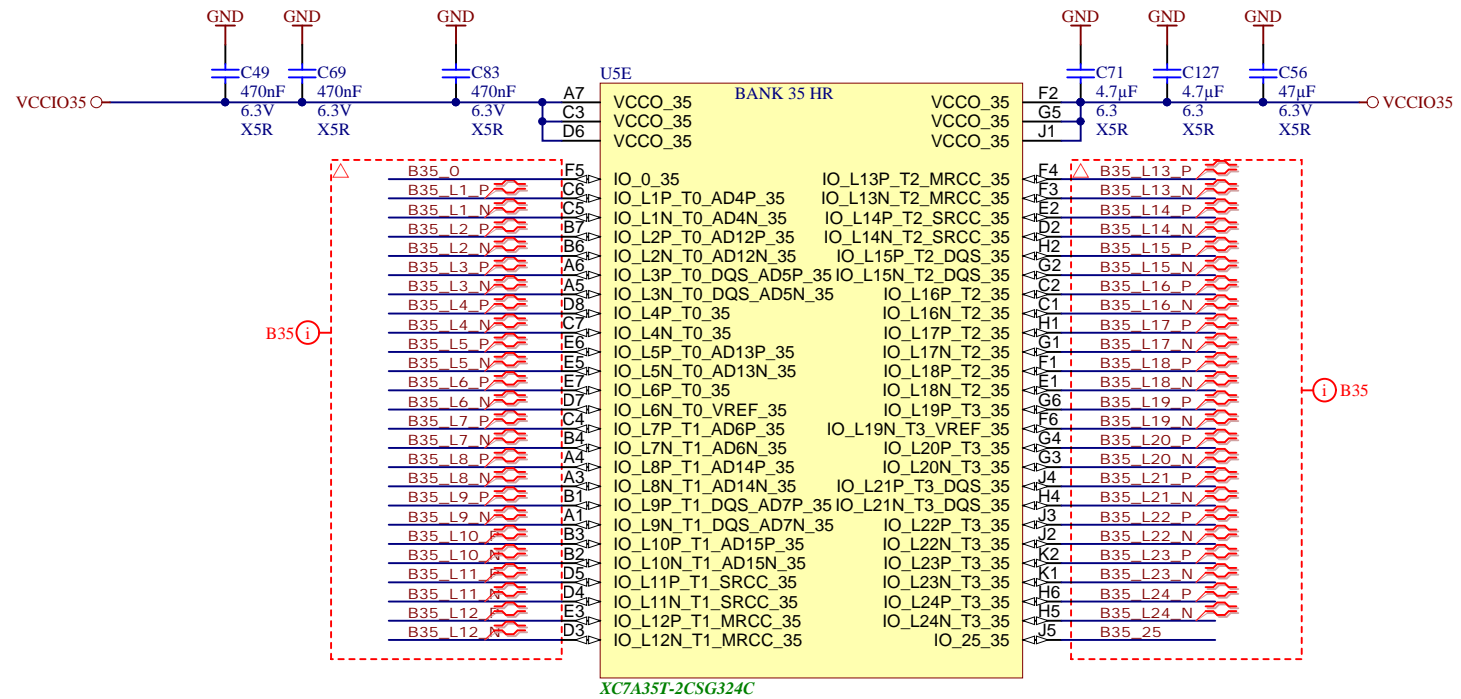

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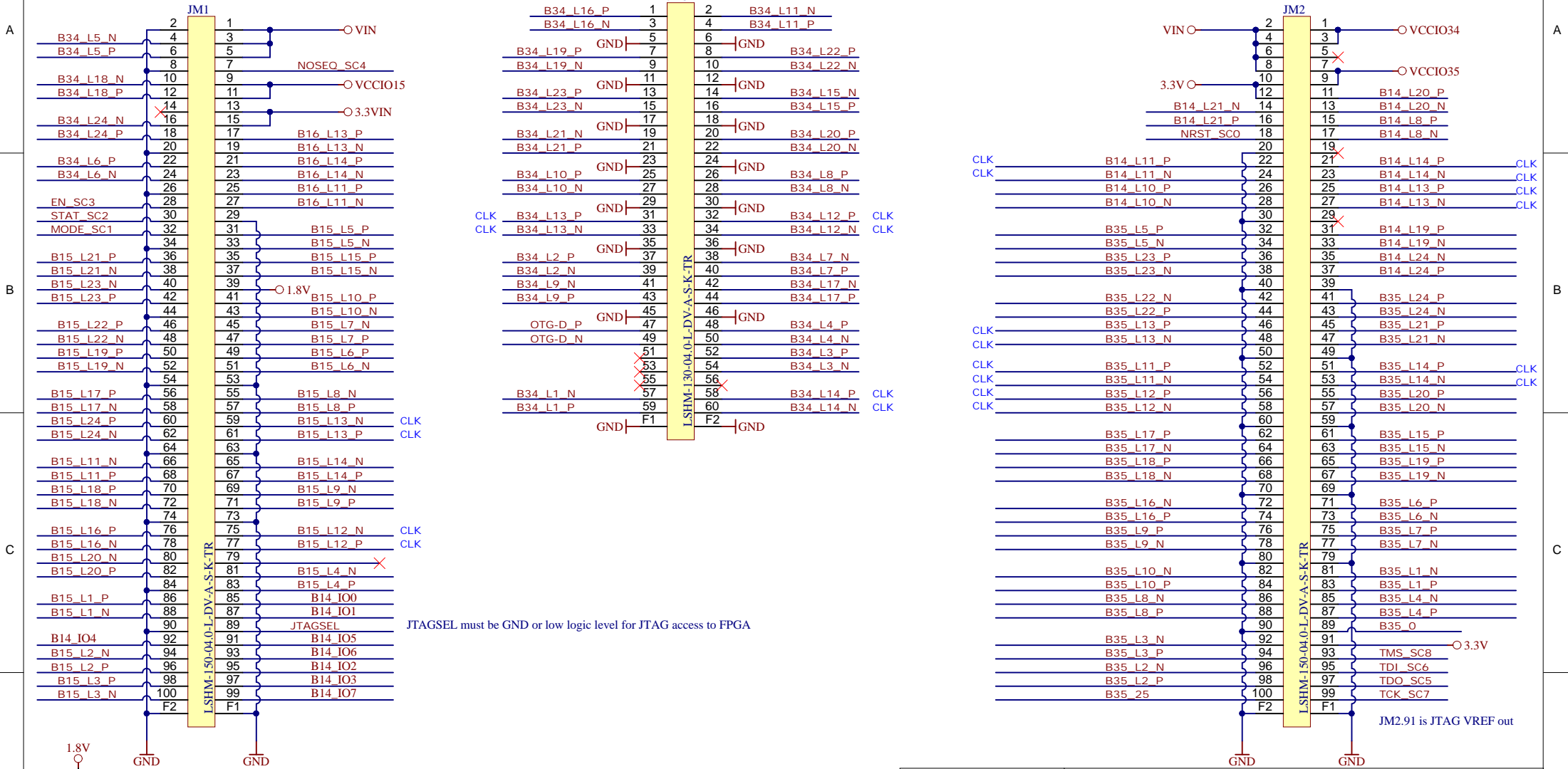



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B16 6 Pins: 3 Differential ; 1.8V Fixed VCCIO
 B15: 48 Pins: 24 Differential; variable VCCIO
 B34: 8 Pins: 4 Differential; variable VCCIO
 B14: 8 Pins: 8 Single ended; 3.3V Fixed VCCIO

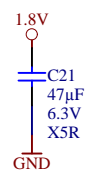
B34: 40 Pins: 20 Differential; variable VCCIO
 USB Device


B35: 50 Pins: 24 Differential; variable VCCIO
 B14: 18 Pins: 9 Differential; 3.3V Fixed VCCIO
 JTAG: 3.3V Levels

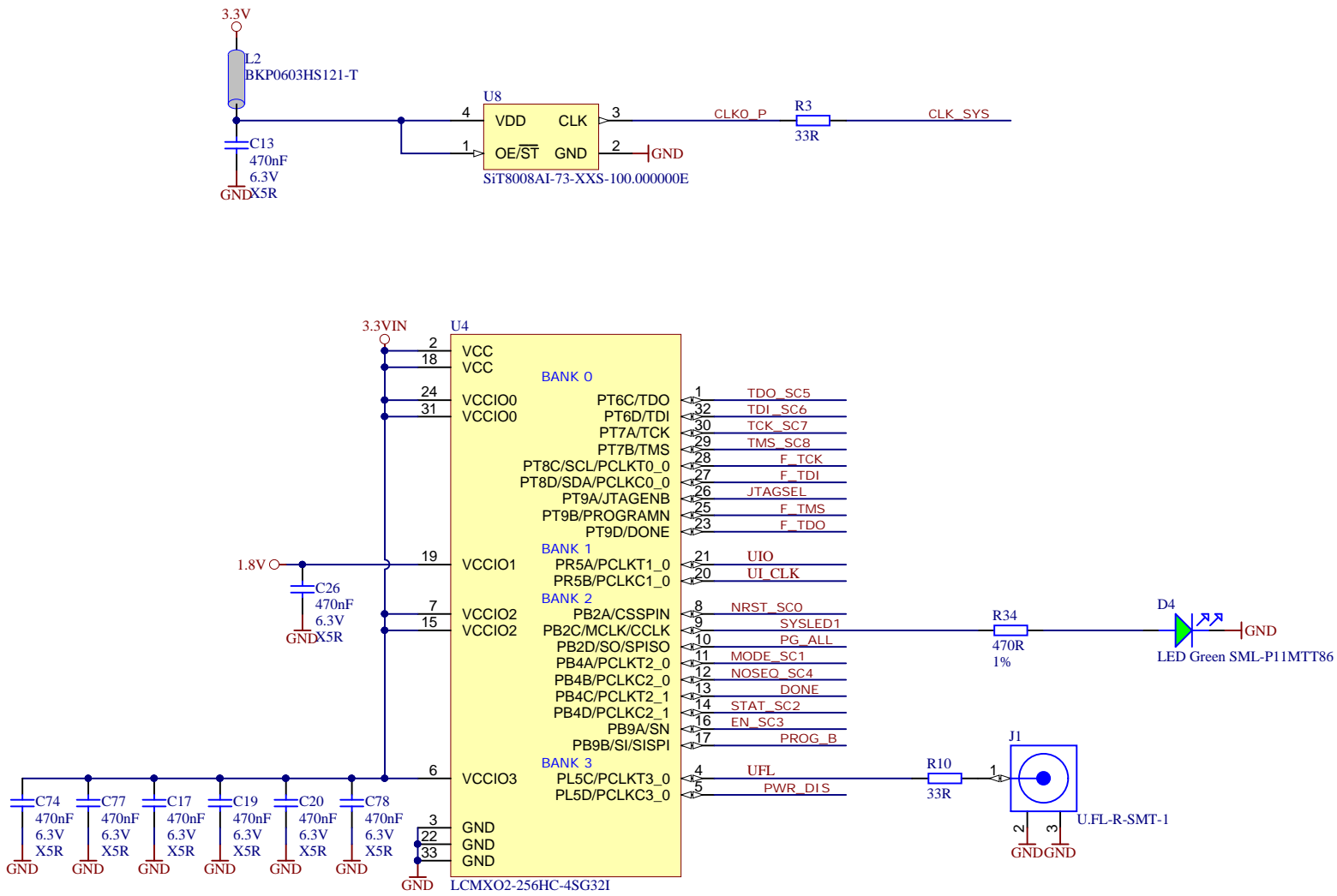


JTAGSEL must be GND or low logic level for JTAG access to FPGA

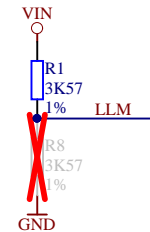
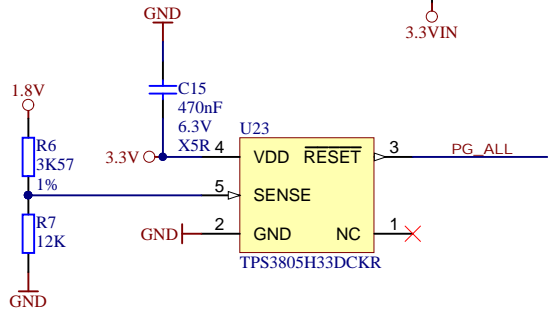
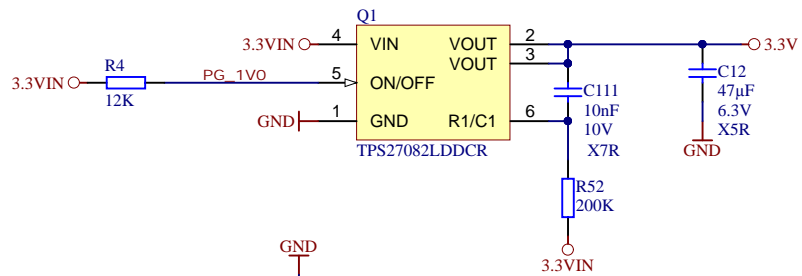
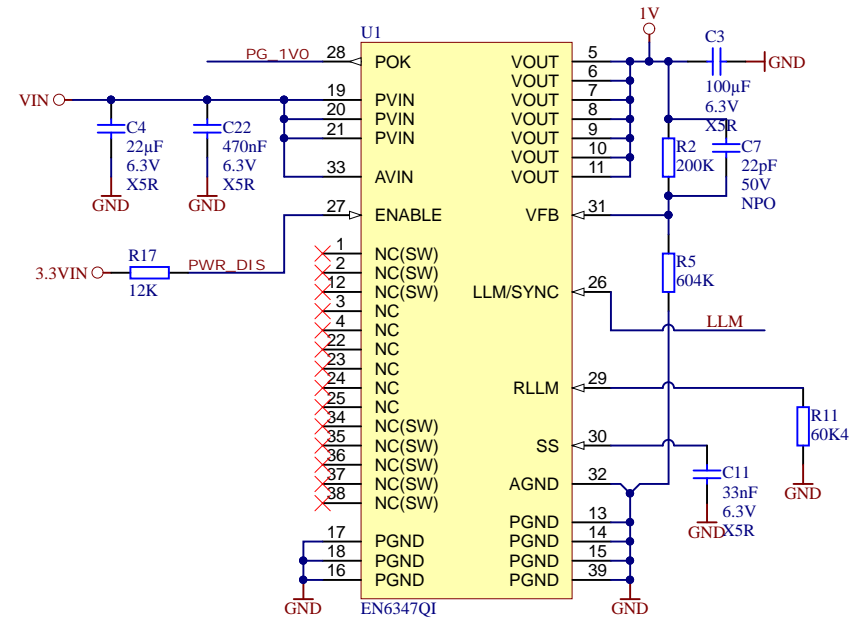
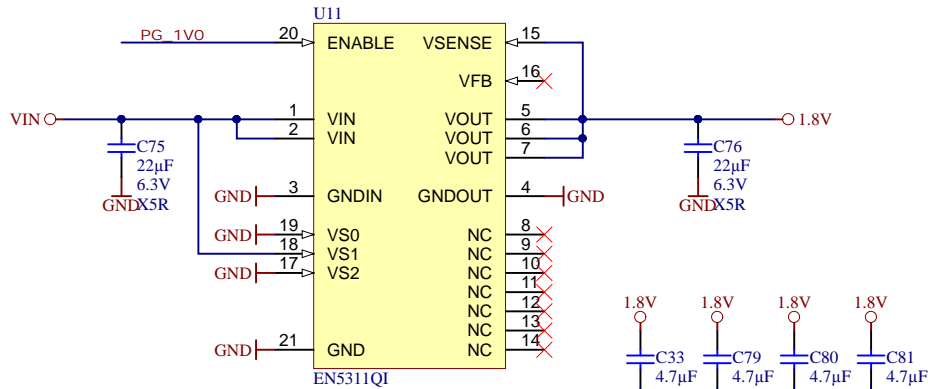
JM2.91 is JTAG VREF out




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