ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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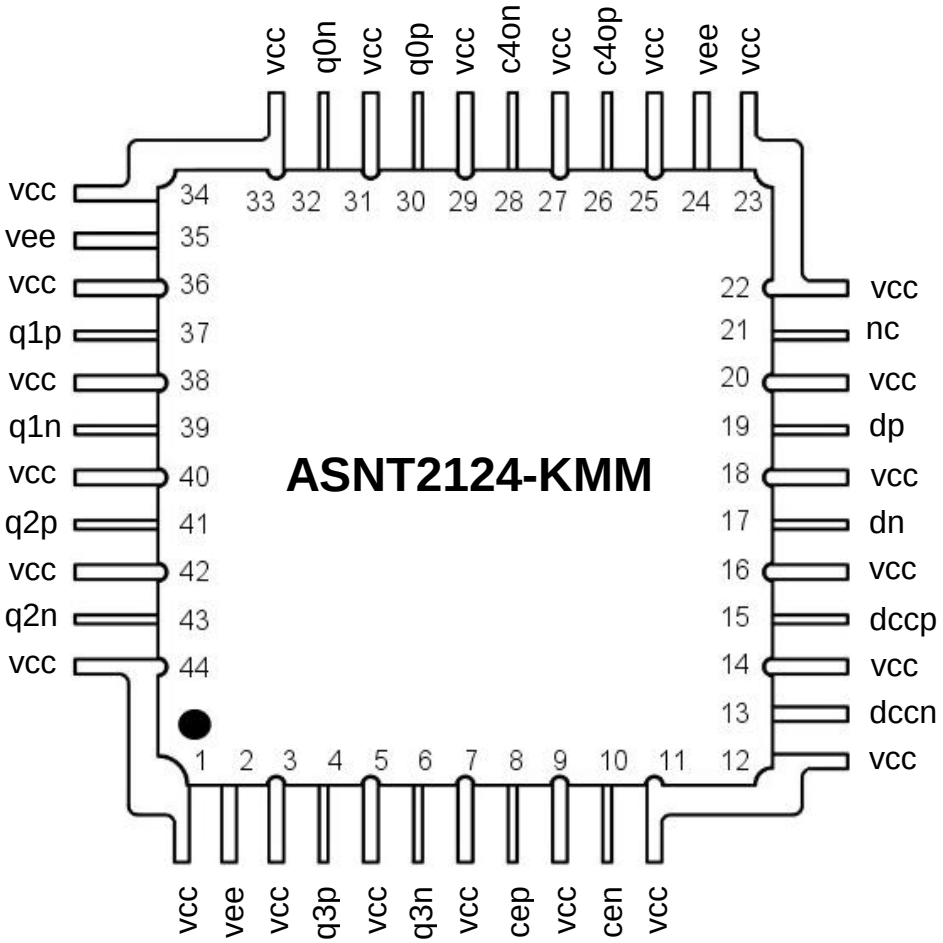
ASNT2124-KMM
DC-64*Gbps* Broadband Digital DDR 1:4 Demultiplexer

- High speed broadband 1:4 Demultiplexer (DMUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Differential CML I/O data and clock buffers
- Half-rate clock input (DDR mode)
- External control of internal clock's duty cycle
- Quarter-rate clock output
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.25*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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DESCRIPTION

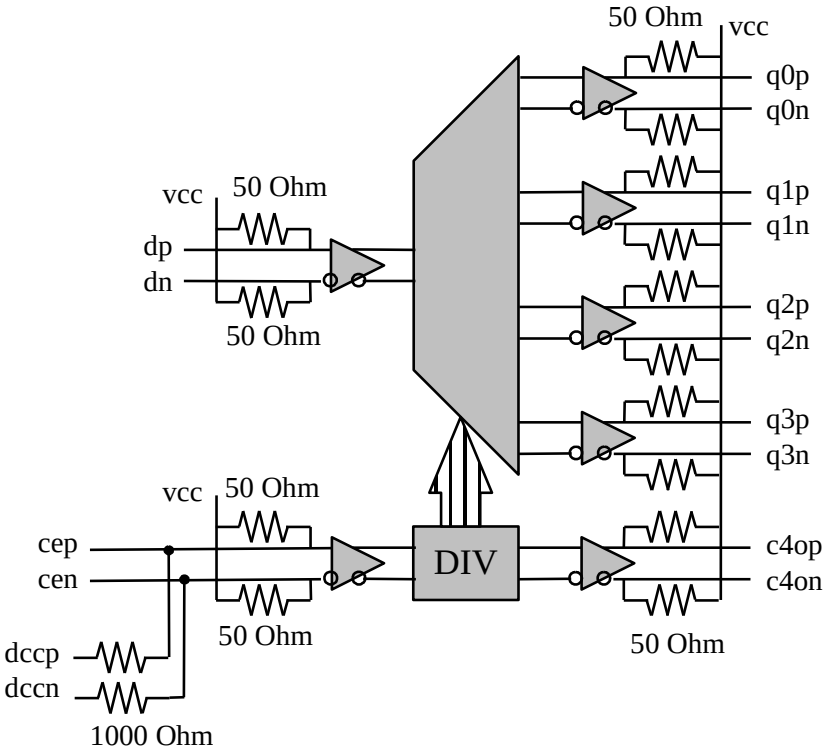

Fig. 1. Functional Block Diagram

ASNT2124-KMM is a low power and high-speed digital 1-to-4 deserializer-demultiplexer (DMUX) that functions seamlessly over data rates (f_{bit}) ranging from DC to its maximum speed.

The main function of the part shown in Fig. 1 is to demultiplex an incoming high speed serial differential CML data bit stream dp/dn running at a bit rate of f_{bit} into 4 parallel data channels q0p/q0n, q1p/q1n, q2p/q2n, q3p/q3n running at a bit rate of $f_{bit}/4$. Differential or single-ended half-rate clock cep/cen must be provided by an external source for the part to function properly. The internal clock's duty cycle can be adjusted through analog ports dccp/dccn.

The parallel words and clock divided-by-4 c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in a very little relative skew over the operating temperature range of the device.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

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HS CIB

The high-speed clock input buffer can accept high-speed clock signals at its differential CML input port cep/cen. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended 50*Ohm* termination to vcc for each input line.

The buffer includes two external DC analog ports dccp and dccn for adjustment of its output signal duty cycle. By lowering the voltage of one of the ports below vcc while keeping the other one at vcc or not connected, the common mode voltage of the corresponding clock input can be lowered below vcc. If both control inputs are left not connected the common mode voltages of both clock inputs are at vcc. The dependence of either input clock common mode voltage on the control voltage is shown in Fig. 2.

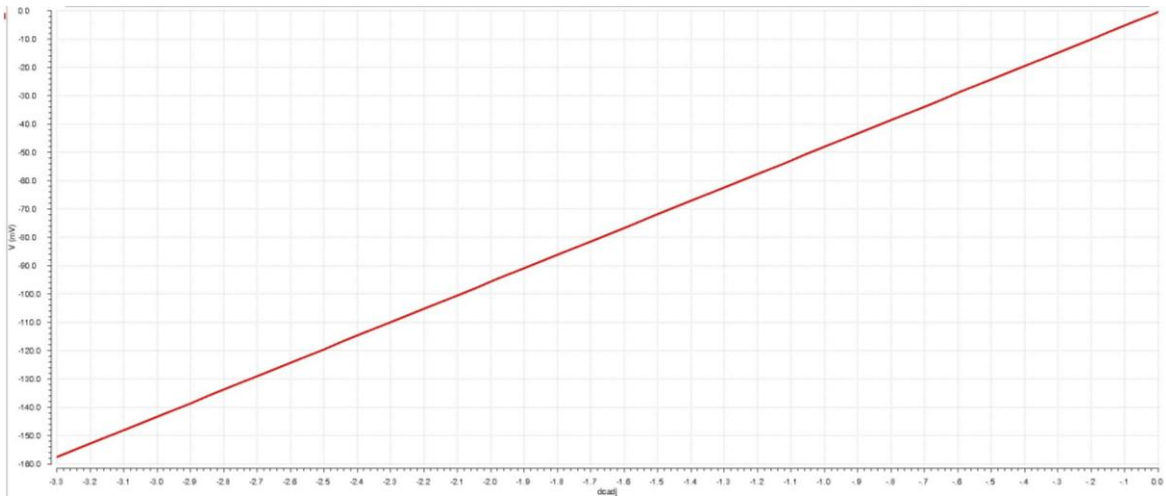

Fig. 2. Dependence of cep (or cen) Common Mode Voltage on dccp (or dccn) Voltage

DMX4:1

The 1-to-4 internal demultiplexer utilizes a tree-type architecture which latches in the serial data stream on both edges of the half-rate clock signal that is supplied by the on-chip divider (DIV). The 4-bit wide data word is then delivered to the data output buffers.

Data OBs

The data output buffers receive high-speed data from DMX4:1 and convert them into differential CML output signals q0p/q0n, q1p/q1n, q2p/q2n, and q3p/q3n. The buffers utilize internal 50*Ohm* loads to vcc and require matching 50*Ohm* external termination resistors to be connected from vcc to each output.

HS COB

The quarter-rate clock output buffer utilizes the same termination scheme as Data OB and can operate at its maximum frequency while producing a full single-ended CML output swing.

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POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.3	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
q0p	30	CML output	Differential quarter-rate data outputs. Require external SE 50*Ohm* termination to vcc
q0n	32		
q1p	37	CML output	
q1n	39		
q2p	41	CML output	
q2n	43		
q3p	4	CML output	
q3n	6		
c4op	26	CML output	Differential quarter-rate clock outputs. Require external SE 50*Ohm* termination to vcc
c4on	28		
High-Speed I/Os			
cep	8	CML input	Differential half-rate clock input signals with internal 50*Ohm* termination to vcc
cen	10		
dp	19	CML input	Differential full-rate data input signals with internal 50*Ohm* termination to vcc
dn	17		
Control Ports			
dccp	15	Analog input	Differential or SE tuning ports with internal SE connections to dp/dn through 1000*Ohm* resistors
dccn	13		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)		1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply (0*V* or -3.3*V*)		2, 24, 35
nc	Not connected pins		21

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		380		*mA*	
Power consumption		1255		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	DC	40	64	*Gb/s*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Half-Rate Input Clock (cep/cen)					
Frequency	DC	20	32	*GHz*	
Differential swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
LS Output Data (q0p/q0n, q1p/q1n, q2p/q2n, q3p/q3n)					
Data Rate	DC	10	16	*Gb/s*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.44		*V*	With external 50*Ohm* DC termination
Output Jitter		2		*ps*	Peak-to-peak at 10*Gb/s*
LS Output Clock (c4op/c4on)					
Frequency	DC	10	16	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Duty Cycle		50		*%*	
Output Jitter		1		*ps*	Peak-to-peak at 10*GHz*
Analog Control Inputs (dccp/dccn)					
Voltage range	vee		vcc	*V*	
Termination		1.0		*KOhm*	to corresponding clock input

PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT2124-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

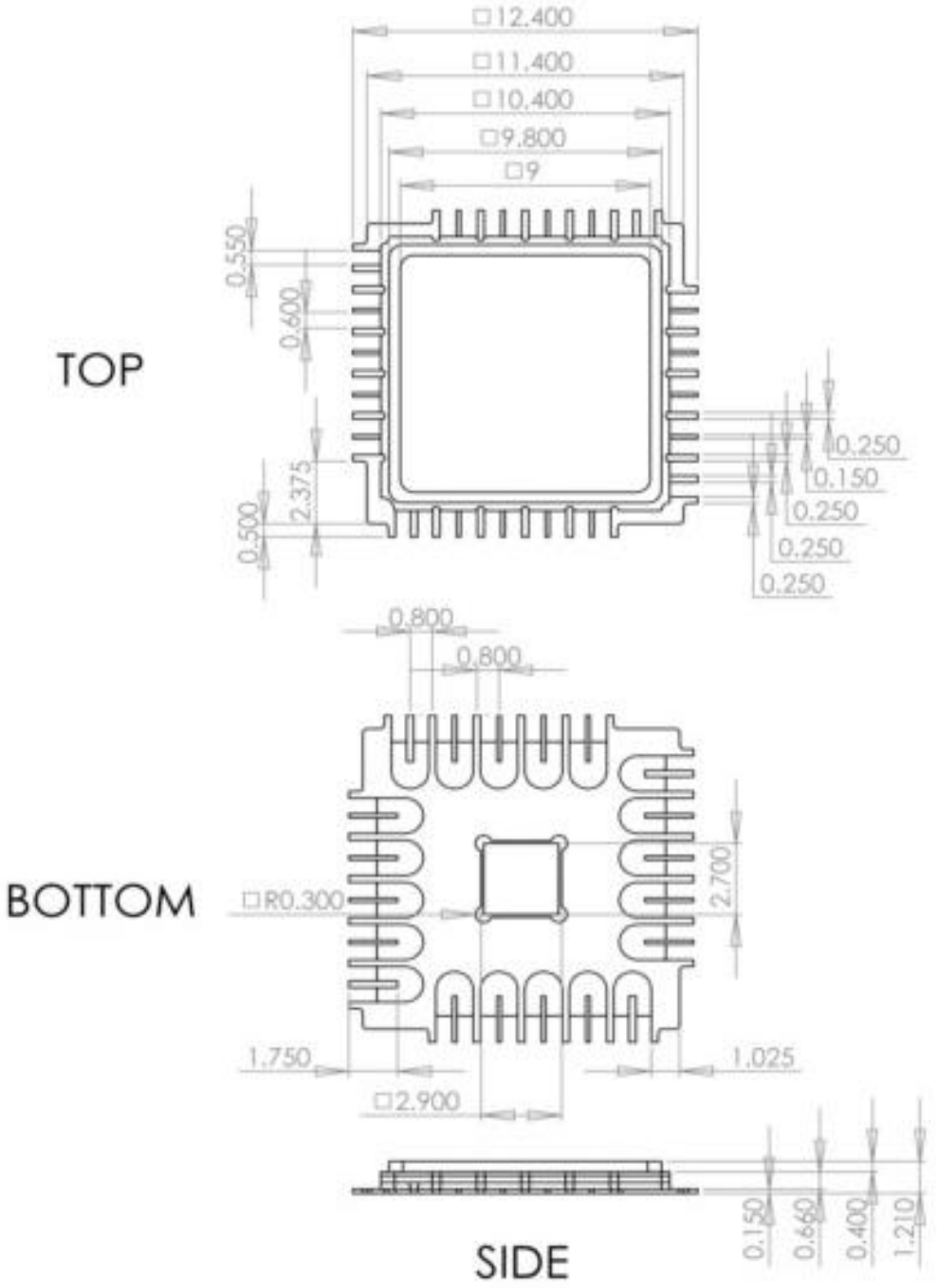

Fig. 3. CQFP 44-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2020	Updated package information
1.1.2	07-2019	Updated Letterhead
1.1.1	05-2016	Corrected pin out diagram Corrected block diagram Corrected the Description section Corrected the HS CIB section Corrected Terminal Functions Corrected Electrical Characteristics Corrected Power Consumption
1.0.1	05-2015	First release
1.0.0	09-2014	Preliminary release