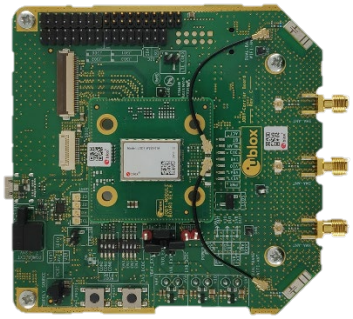
EVK-JODY-W3

Evaluation kit for JODY-W3 host-based modules

User guide



Abstract

This document describes how to set up the EVK-JODY-W3 evaluation kit to evaluate JODY-W3 series multiradio modules with Wi-Fi and Bluetooth.

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C1 – Public

Document information

Title	**EVK-JODY-W3**
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This document applies to the following products:

Product name	Type number	Firmware version	PCN reference
EVK-JODY-W374	EVK-JODY-W374-00A-00		N/A
EVK-JODY-W377	EVK-JODY-W377-00A-00		N/A

Contents

1 Kit description

JODY-W3 series modules provide complete short-range transceiver solutions based on the NXP chipset 88Q9098.

Intended for the most advanced in-car infotainment and connectivity systems, JODY-W3 series modules deliver the highest data rates in Wi-Fi using advanced Wi-Fi 6 802.11ax technology. The modules operate in concurrent dual-bands, Wi-Fi 2.4 and 5 GHz, dual-MAC, and 2x2 MIMO, and support Bluetooth 5.1 features like extended advertising, long range, and 2 Mbit/s (PHY) data rates.

The modules require a host processor running Linux or Android and connect to the host processor through either PCIe or SDIO for Wi-Fi, SDIO or high-speed UART for Bluetooth, and PCM/I2S for Bluetooth audio.

EVK-JODY-W3 allows an external host processor to access several practical features for testing and evaluating the Wi-Fi and Bluetooth connectivity supported in JODY-W3 series modules, including:

- External connectors to all host interfaces (PCIe, SDIO and UART)
- USB interface to easily access the Bluetooth UART interface via a USB-to-UART bridge
- Digital and analog audio interfaces for Bluetooth
- Two internal dual-band 2.4/5 GHz antennas for Wi-Fi and Bluetooth.
- Three SMA connectors for external antennas.
- GPIO pins and other module interfaces are accessible through pin headers
- Multiple power supply options

For more information about JODY-W3 modules, see the JODY-W3 series data sheet [1] and system integration manual [2].

1.1 Overview

Table 1 lists the available evaluation kit versions:

Evaluation kit	Ordering code	Description	Suitable for evaluation of
EVK-JODY-W374	EVK-JODY-W374-00A	Evaluation kit for JODY-W374 Two antenna pins for simultaneous dual-band 1x1 2.4 GHz and 2x2 5 GHz Wi-Fi and Bluetooth 5.1	JODY-W374-00A
EVK-JODY-W377	EVK-JODY-W377-00A	Evaluation kit for JODY-W377 Three antenna pins for simultaneous dual-band 2x2 2.4/5 GHz Wi-Fi and Bluetooth 5.1	JODY-W377-00A

Table 1: Available EVK-JODY-W3 evaluation kits

Figure 1 shows the EVK-JODY-W3 evaluation board and its main connectors.

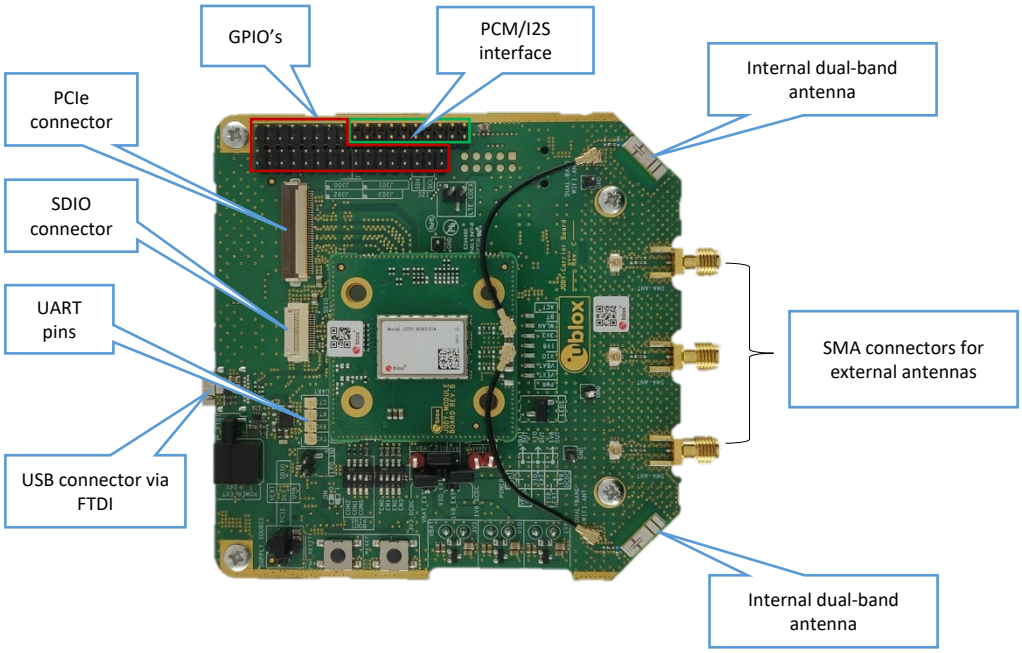


Figure 1: EVK-JODY-W3 outline showing main connectors

The EVK-JODY-W3 design is split into a module board and a carrier board. The module board includes the JODY-W3 series module and u.FL antenna connectors directly accessing the antenna pins on the module. The bigger carrier board hosts the module board and includes all the necessary connectors for connecting the JODY-W3 series module to the host system.

1.2 Kit includes

Table 2 shows the various components included in the EVK-JODY-W3.

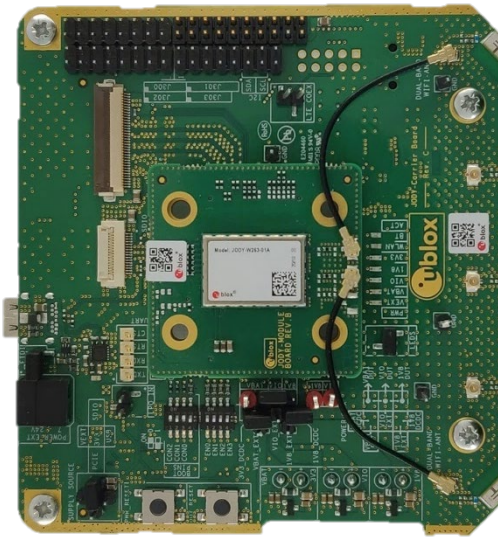
Part	Description	Outline
Evaluation board (EVB)	Evaluation board for the JODY-W3 series modules. The board includes SMA antenna connectors that connect to external antennas for Wi-Fi and Bluetooth. EVK-JODY-W3 also supports two internal dual-band Wi-Fi/Bluetooth antennas.	
M.2 PCIe to ZIF adapter	M.2 PCIe to ZIF adapter for Wi-Fi host communication. One ZIF flat cable is included for both PCIe adapters.	
Mini-PCIe to ZIF adapter	Mini-PCIe to ZIF adapter for Wi-Fi host communication. One ZIF flat cable is included for both PCIe adapters.	
Micro SDIO to ZIF adapter and flat cable	Micro SDIO to ZIF adapter and flat cable for Wi-Fi and/or Bluetooth host communication. The adapter is compatible with host sockets designed for micro SD memory cards.	
Type-C USB cable	Type-C USB cable for Bluetooth host communication over UART connected via FTDI.	
External antennas	2 x Dual band Wi-Fi/Bluetooth antenna, Linx Technologies ANT-DB1-RAF-SMA	

Table 2: EVK-JODY-W3 component list

1.3 Software

The software package including the reference driver from NXP is only distributed to customers that have signed a Limited Use License Agreement (LULA-M) with u-blox. For information about how to obtain the driver package, contact your local u-blox support team. The software package and additional documentation can also be obtained directly from NXP.

A Yocto/OpenEmbedded meta layer, which includes recipes for integrating the drivers into Yocto-based projects, can be provided on request by u-blox.

Refer to the JODY-W3 system integration manual [2] for a description of the available driver packages and basic usage examples.

1.4 System requirements

The evaluation kit has the following system requirements:

- Host (PC or embedded system) with
  - Mini-PCIe or M.2 Key E slot for access to Wi-Fi through the PCIe host interface
  - Micro SDIO slot for access to Wi-Fi through the SDIO host interface
  - USB 2.0 interface for access to the Bluetooth UART interface through USB-to-UART bridge
- Supported operating systems
  - Linux (3.x/4.x/5.x)
  - Android Pie (9.0.0_2.3.4)

2 Specifications

This section includes the different operating parameters for the EVK-JODY-W3.

2.1 Operating conditions

Table 3 describes the absolute range for key EVK operating parameters.

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	Power supply voltage	3.14	3.3	3.46	V
VIO	I/O supply voltage 1.8 V	1.71	1.8	1.89	V
	I/O supply voltage 3.3 V	3.14	3.3	3.46	V
1V8	Analog power supply voltage 1.8 V	1.71	1.8	1.89	V
T_A	Ambient operating temperature	-40	-	+85*	°C
Ripple Noise	Peak-to-peak voltage ripple on all supply lines.	-	-	30	mV

Table 3: EVK-JODY-W3 operating conditions

☞ The signal voltage for the SDIO interface of the JODY-W3 series module is powered from the **1V8** supply. A level shifter is required to operate the module in Default Speed and High-Speed modes at 3.3 V signal voltage [3]. For further information contact your local u-blox support team.

3 Getting started

This chapter describes the basic settings and procedures necessary to get started with the JODY-W3 EVK.

☞ Figure 1 shows an overview of the EVK and its main connectors. For more detailed description of the available connectors and configuration options, see section 4 .

Follow the procedure below to evaluate JODY-W3 series module using EVK-JODY-W3:

1. Connect the internal or external antennas to the EVK:
   - EVK-JODY-W374 uses the two internal dual-band antennas by default for any Wi-Fi and Bluetooth communication.
   - EVK-JODY-W377 uses one of the internal antennas by default for Bluetooth, and Wi-Fi is configured to use SMA connectors.
   - The two included external antennas connect to the selected SMA connectors, SMA1 and SMA2, on the EVK-JODY-W377 board.

☞ For more information about the antenna configuration, see also section 4.10

2. Set DIP switch SW503 to select the host interfaces for Wi-Fi and Bluetooth from the possible combinations PCIE-UART, SDIO-UART or SDIO-SDIO, as described in section 4.9.
3. Configure the power supply source as described in section 4.3 and shown in Table 5. The most common configuration uses the Wi-Fi host interface as the supply source, which can be either PCIe or SDIO.
4. Connect the host interfaces to the host system. The EVK and supplied PCIe and SDIO adapters use zero insertion force (ZIF) connectors and flat cables for connecting the adapters. To connect the cable, gently flip up the small locking flap of the connector, align and insert the flat cable with the blue marking pointing upwards, and then close the locking flap.
   - For PCIe connection, choose either the M.2 or the mini-PCIe adapter depending on the available connector on the host platform. First, plug the adapter into the PCIe connector on the host system and then connect it with the flat cable to the connector (J203) on the EVK, as shown in Figure 2. The PCIe interface can be used for Wi-Fi communication with the JODY-W3 series

module.

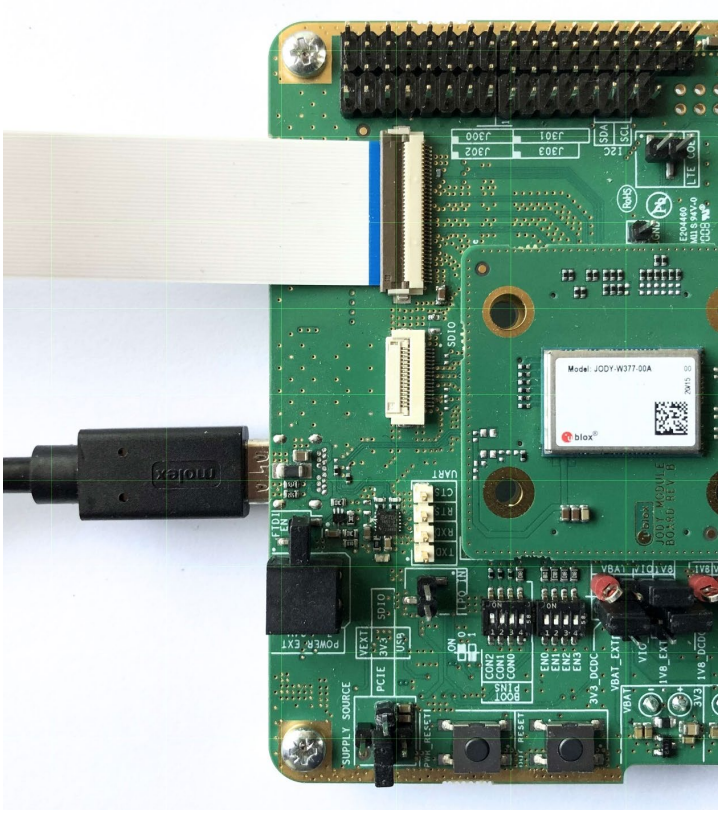


Figure 2: PCIe and USB connectors

- For SDIO connection, connect the micro SDIO adapter card with the flat cable to the SDIO connector (J204) on the EVK as shown in Figure 3 and insert the adapter card into an SDIO connector of the host system. The SDIO interface can be used for Wi-Fi, and optionally

Bluetooth, communication with the JODY-W3 series module.

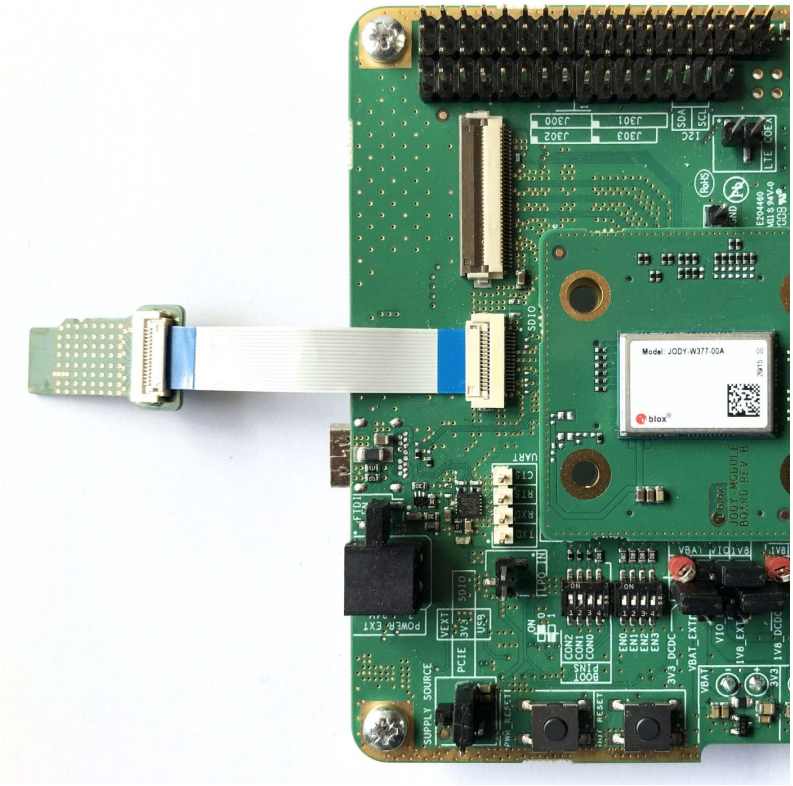


Figure 3: SDIO connector

- A high speed UART interface can be used for Bluetooth communication with the JODY-W3 series module. A USB-to-UART bridge is included on the evaluation board. To use the Bluetooth interface through USB, connect the included USB cable to the USB type-C connector on the EVK (see Figure 2) and connect it to a USB interface on the host system. Make sure that jumper J400 is bridged (default setting) to enable Bluetooth communication over USB. Refer to section 4.6 for information how to access the UART interface for Bluetooth directly.

5. Power on the host system. The LEDs on the EVK for the different voltage levels should turn green to indicate proper power supply. At this point the module should be detected by the host system.
6. Install the necessary driver software for the JODY-W3 series module as described in the System integration manual [2].

4 Board description

This section describes the logical components, connectors, jumpers and switches used to configure the EVK-JODY-W3.

4.1 Block diagram

Figure 4 shows the block diagram of the EVK with the different peripheral connectors around it.

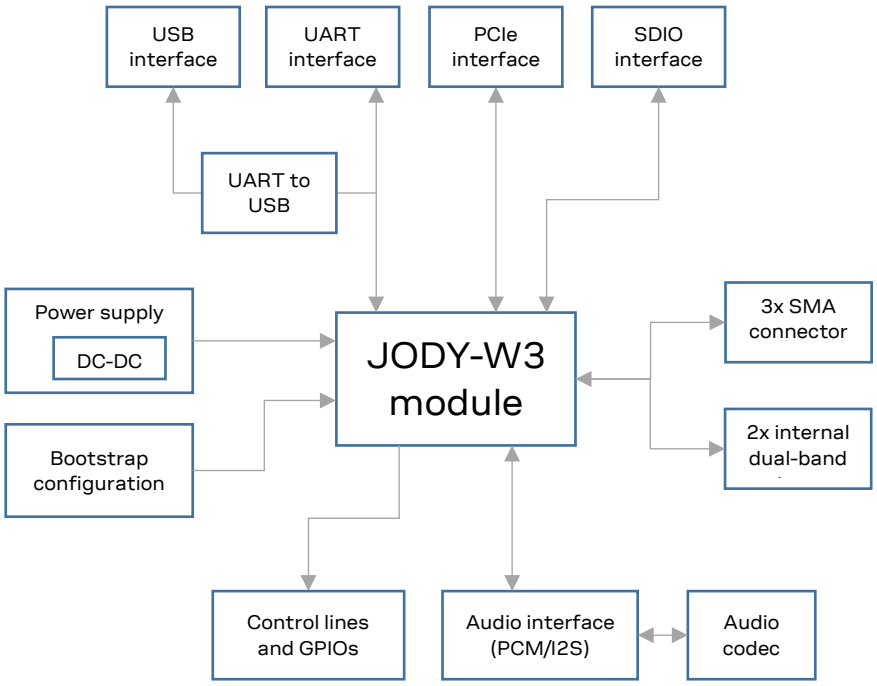


Figure 4: EVK-JODY-W3 block diagram

4.2 Overview of jumpers and connectors

Figure 5 shows an overview of the evaluation board and its connectors. The EVK makes all the interfaces of the JODY-W3 series module accessible through connectors or pin headers. The available interfaces and configurations options are described in detail in the following sections.

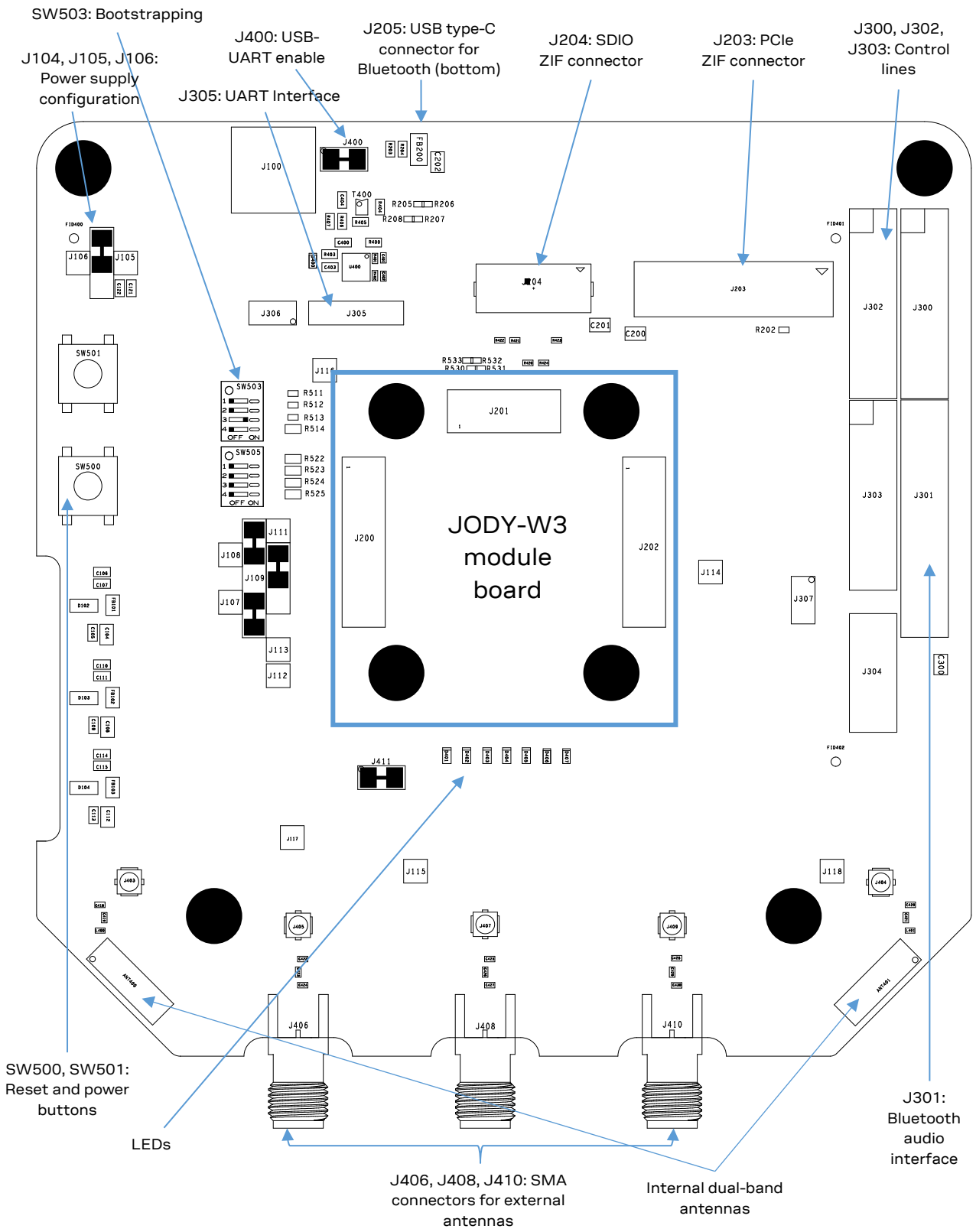


Figure 5: EVK-JODY-W3 jumpers and connectors

Table 4 provides a summary of the connectors and jumpers used to configure EVK-JODY-W3.

Designator	Connector	Description
J104, J105, J106	Power supply configuration	Jumper settings for DC-DC input power supply configuration (4.3.1)
J107, J108, J109, J111	Input voltage configuration	Jumper settings for selecting the input voltage for the module from power supply configuration (4.3.2)
J203	PCIe connector	ZIF connector for PCIe host interface on EVK (4.4)
J204	Micro SDIO connector	ZIF connector for SDIO host interface on EVK (4.5)
J305	Bluetooth UART	UART connector for Bluetooth host interface (4.6)
J205	Type-C USB	USB connector for Bluetooth host interface (via USB-to-UART bridge) (4.6)
J301	Blueooth audio	Connector for the PCM/I²S audio interface (4.7)
J300, J302, J303	Control lines	Connector for host and device wake for Bluetooth and Wi-Fi (4.8)
SW503	Bootstrapping	Pin headers for host interface selection (4.9)
J400	USB-UART Enable	Jumper to enable/disable the Bluetooth host interface via USB-to-UART bridge
J406, J408, J410	SMA connectors	SMA coaxial RF connectors for external antennas (4.10)

Table 4: JODY-W3 evaluation board connectors

4.2.1 Jumper conventions

Figure 6 shows the graphical conventions used for jumper settings illustrated in this document. Pin 0 is shown in grey color. All jumpers are shown with red lines terminated with round edges.

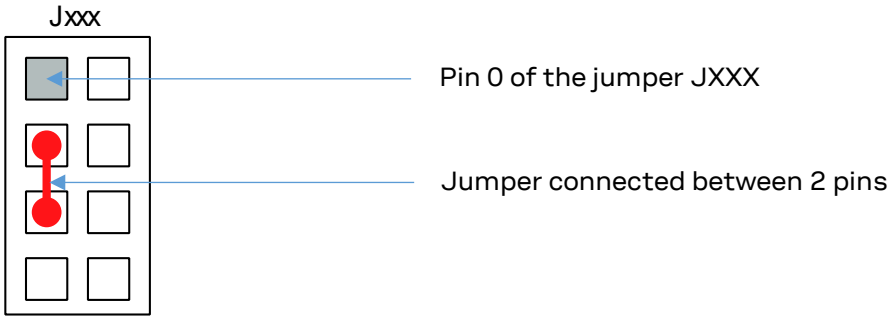


Figure 6: Jumper convention

4.3 Power supply configuration

JODY-W3 series modules are supplied with 3.3 V (**3V3**), 1.8 V (**1V8**) and a **VIO** voltage that can be either 3.3 V or 1.8 V. Power supply for the EVK can be provided over the different host interfaces or from external sources. The following power supply options are available on the EVK:

- PCIe, SDIO, USB interfaces: The EVK is powered through the host interface. All internal voltages are generated by DC-DC converters on the EVK.
- External power supply (VEXT): EVK-JODY-W3 can be connected to an external power supply of 7 V to 24 V. DC-DC converters are used for generating all the required internal voltages.
- Individual supply: All the individual voltage rails **3V3**, **1V8** and **VIO** are supplied from external power sources.

Figure 7 describes the external power supply connectors and jumpers to configure the different power supply options.

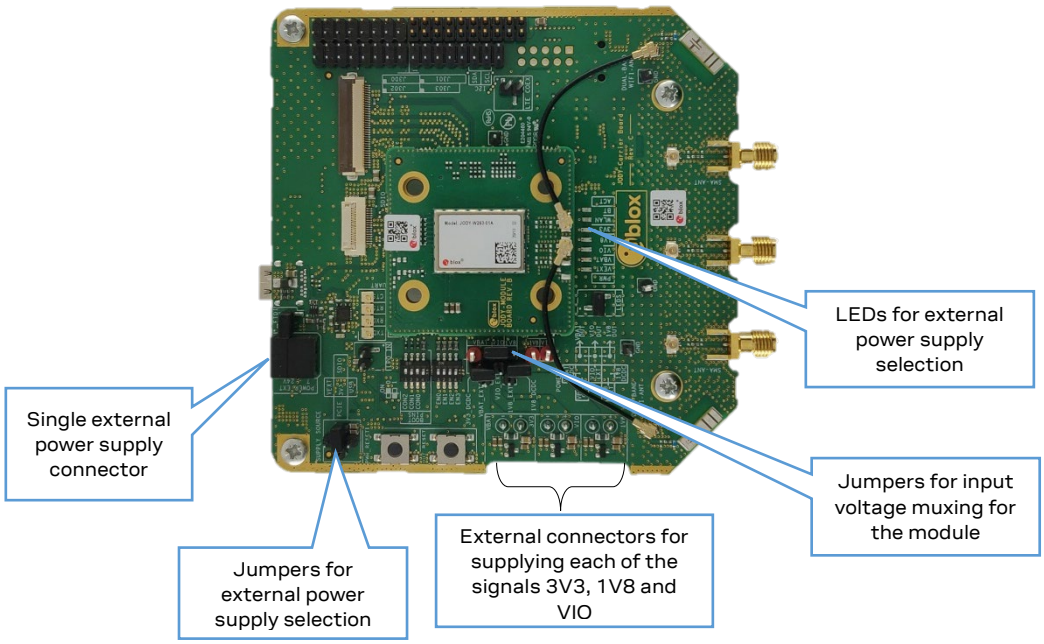


Figure 7: Overview of EVK power supply configuration

Figure 8 shows the power supply tree for the EVK.

☞ The **VBAT** rail on the EVK is used for the **3V3** supply of the JODY-W3 module.

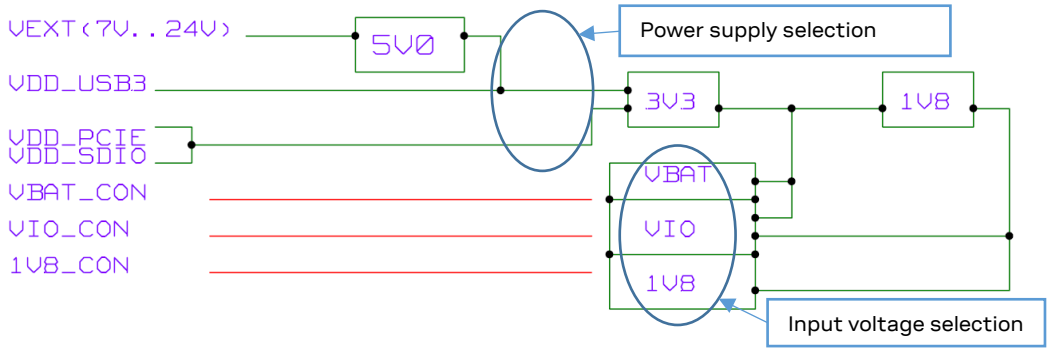


Figure 8: JODY-W3 EVK power supply tree

Figure 9 shows the external input power supply selection using the jumpers J104-J106 and the input voltage selection for the JODY-W3 module using the jumpers J107-J110. The detailed settings are further described in Table 5 and Table 7.

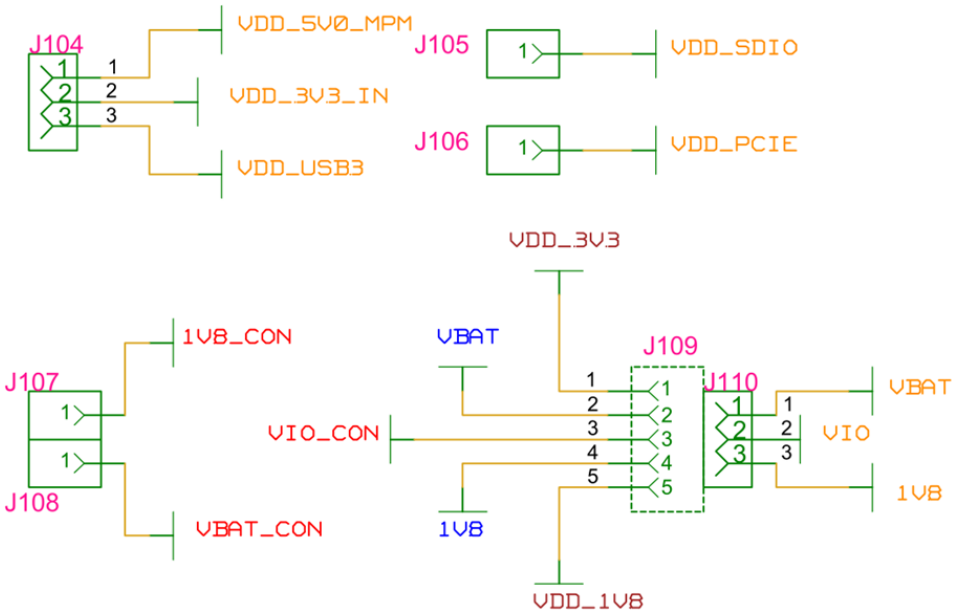


Figure 9: Power supply and input voltage selection

4.3.1 Power supply selection

The selection for the external power supply sources is shown in Figure 10.

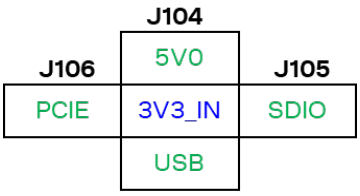
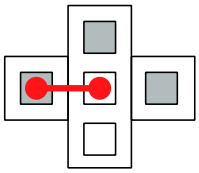
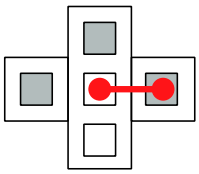
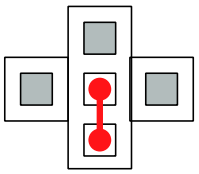


Figure 10: External power supply sources

3V3_IN is the input to the DC-DC converters on the EVK to generate the 3.3 V and 1.8 V voltages. The jumpers J104-J106 are used to select to external power supply input for the EVK. The available options are shown in Table 5.

Power supply source	Jumper configuration
3.3 V from PCIe interface Use the M.2 or mini-PCIe adapter with the flat cable to connect to the host system.	
3.3 V from SDIO interface Use the micro SDIO adapter with the flat cable to connect to the host system.	
5 V from USB interface Use the Type-C USB cable to connect to the host system. Note: The USB host port must be able to deliver a current of up to 1000 mA for Wi-Fi operation. The current provided by a standard USB 2.0 interface is sufficient for Bluetooth-only operation.	

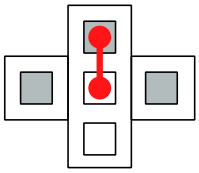
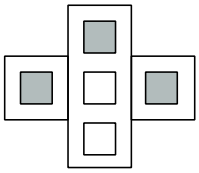
Power supply source	Jumper configuration
7 V – 24 V external power supply External supply (7 V – 24 V) must be connected to the power jack J100. The external supply voltage is first converted to 5 V using a DC-DC on the EVK. J100: Phoenix Contact 1721986	
All input voltages supplied from individual sources External supplies must be connected to the power jacks located on the bottom side of the EVK for 3V3 (J101), 1V8 (J103) and VIO (J102). J101-J103: Phoenix Contact 1721986	

Table 5: Jumper settings for power supply selection for the EVK

4.3.2 Input voltage selection

With reference to the power matrix shown in Figure 11, position jumpers J107, J108, J109, and J111 to select the appropriate input voltages for the module. The jumpers configure the input between DC-DC generated voltages and the direct input voltage from the individual supplies.

Figure 11 shows the jumper pins for configuring the input voltages described in Table 6.

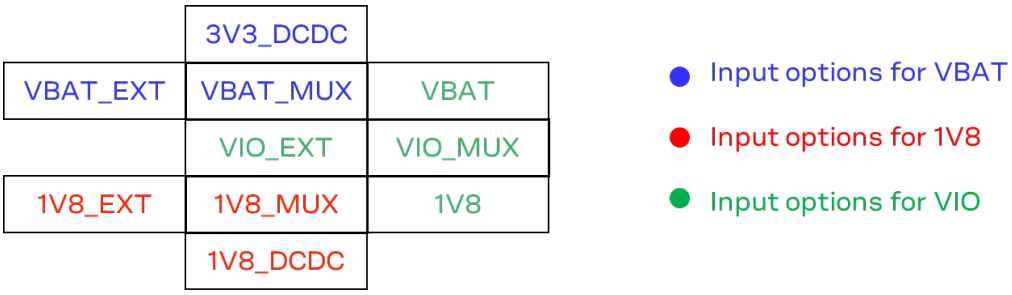
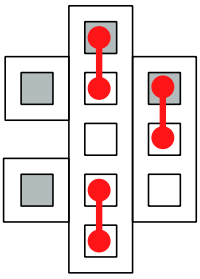
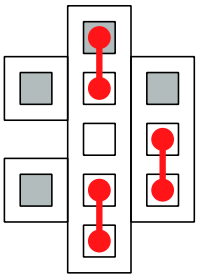


Figure 11: Input voltage pins

Designator	Module supply	Source
VBAT_MUX	3V3	Can be connected to 3V3_DCDC or VBAT_EXT
VIO_MUX	VIO	Can be connected to VBAT, 1V8 or VIO_EXT
1V8_MUX	1V8	Can be connected to 1V8_DCDC or 1V8_EXT

Table 6: Input voltage options

For the operation of EVK-JODY-W3, power supply jumpers must be set as explained in Table 5 and Table 7. The first one selects the external power supply and the second one defines the voltage levels to operate the module. Table 7 describes the different options to select the input voltages for the module.

Jumper settings	Description / Voltage levels
 VIO (3.3 V)  VIO (1.8 V)	Power supply using host interface (PCIe, SDIO or USB) or single external supply (VEXT) and DC-DC generated voltages. VIO voltage is derived from either 1V8 or VBAT. • 3V3/VBAT – 3.3 V • 1V8 – 1.8 V • VIO – 1.8 V or 3.3 V

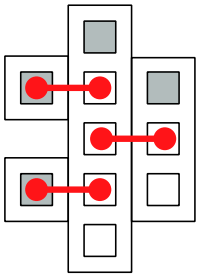
	Power supply using individual external input sources for each of the voltage rails 3V3, 1V8 and VIO. External supplies are connected at the bottom of the EVK carrier board. Note: VIO can also be connected to VBAT or 1V8 to supply it from the same external 3.3 V or 1.8 V source.

Table 7: Jumper settings for input voltage selection

4.4 PCIe interface

The EVK can be connected through a PCIe connector for Wi-Fi communication with the host system. Adapters for M.2 Key E and mini-PCIe connectors on host side are included in the kit. The PCIe host interface connector (J203) is shown in Figure 12.

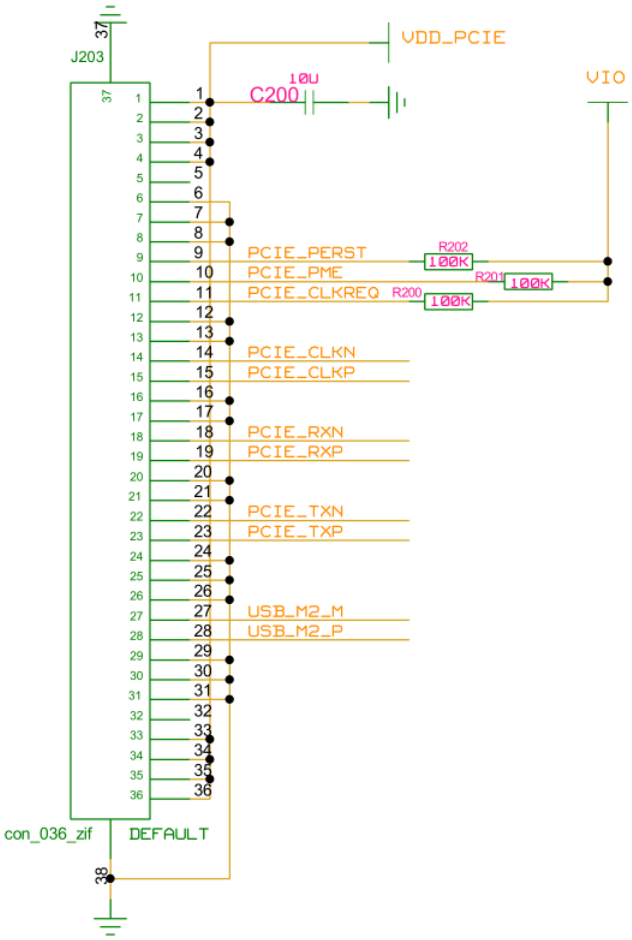


Figure 12: PCIe interface connector

VDD_PCIE is connected to the power supply connector (J106) and is used for supplying 3.3 V for **VBAT** from the PCIe interface.

4.5 SDIO interface

The EVK can be connected through a micro SDIO connector for Wi-Fi communication with the host system. The SDIO connector can optionally be used for Bluetooth. The SDIO host interface connector (J204) is shown in Figure 13.

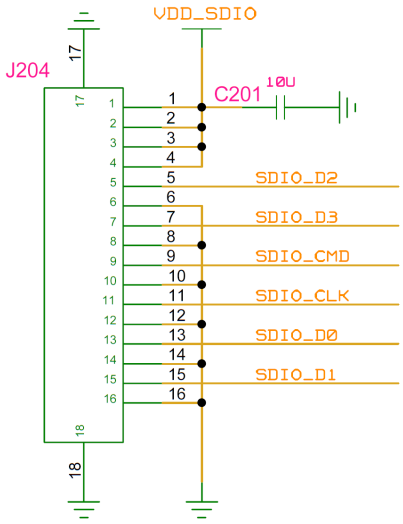


Figure 13: SDIO interface connector

All signals except **VDD_SDIO** are directly connected to the JODY-W3 module through 22 Ω series resistors connected on the module board.

VDD_SDIO is connected to the power supply connector (J105) and is used for supplying 3.3 V for **VBAT** from the SDIO interface. The SDIO interface has 50Ω impedance. The SDIO signals are powered by the **1V8** voltage domain.

Pull-up resistors for the SDIO lines are not installed on the EVK because they are typically included in the host CPU. The EVK carrier board has the provision to install pull-up resistors if needed by the design.

4.6 Bluetooth UART interface

The Bluetooth UART interface of the JODY-W3 series module can be accessed either directly through the UART pins on J305, or through the USB type-C connector via a USB-to-UART bridge (default).

A USB-to-UART bridge (FTDI FT234XD) is included on the evaluation board to connect to the high speed UART interface of the JODY-W3 series module. **VDD_USB** from the USB connector is converted by a DC-DC to 3.3 V and connected to the power supply connector (J104) for supplying **VBAT** from the USB interface. Place the jumper on J400 to use Bluetooth through the USB type-C connector.

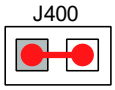


Figure 14: Jumper setting to use Bluetooth over USB

The 4-pin UART interface of the JODY-W3 series modules can be directly accessed through the Bluetooth UART connector J305. To use the UART interface directly, remove the jumper on J400 and connect the UART host interface to the respective module side pins on J305 as shown in Figure 15 and Table 8. Signal ground can be connected to one of the available GND pins on J303 as shown in Figure 18. The UART signals are powered by the **VIO** voltage domain.

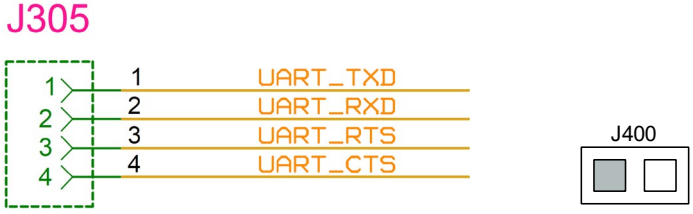


Figure 15: Bluetooth over UART interface

Name	I/O	Description	Remarks
UART_TXD	O	UART TX signal	Connect to Host RX
UART_RXD	I	UART RX signal	Connect to Host TX
UART_RTS	O	UART RTS signal	Connect to Host CTS
UART_CTS	I	UART CTS signal	Connect to Host RTS

Table 8: UART signal description

4.7 Bluetooth audio interface

A MAX9860 16-bit audio codec for Bluetooth voice applications is provided on the JODY-W3 EVK and connected to the PCM/I2S interface of the module. A 3.5 mm audio jack (J206) to connect a headset is available on the bottom side of the EVK. The codec is operated with a master clock (MCLK) of 19.2 MHz. The MAX9860 audio codec is completely controlled through software using an I2C interface. The codec responds to the I2C slave address 0x20 for all write commands and 0x21 for all read operations.

Place jumpers J401 and J402 on the bottom side of the EVK to enable the audio codec.

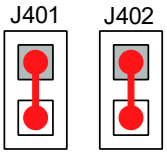


Figure 16: Jumpers to enable the audio codec

The I2C interface of the audio codec is provided on connector J303 of the EVK as shown in Figure 17 and Table 9.

The PCM/I2S interface of the JODY-W3 module is directly connected to the serial audio interface of the MAX9860 audio codec. The PCM pins are shared with the I2S interface and are additionally provided on connector J301 as shown in Figure 18 and Table 9.

Name	I/O	Connector / pin no.	Description
I2C_SDA	I/O	J303 / 11	I2C Serial-Data Input/Output
I2C_SCL	I	J303 / 13	I2C Serial-Data clock
PCM_CLK	I/O	J301 / 16	PCM clock Alternate function: I2S clock
PCM_SYNC	I/O	J301 / 15	PCM frame sync Alternate function: I2S word select
PCM_IN	I	J301 / 18	PCM data in Alternate function: I2S data in
PCM_OUT	O	J301 / 17	PCM data out Alternate function: I2S data out

Table 9: Audio interfaces

4.8 Other interfaces

Connectors J301 (Figure 18) and J303 (Figure 17) provide several other interfaces from the JODY-W3 series module, such as host wake-up signals, GPIOs, and audio interfaces.

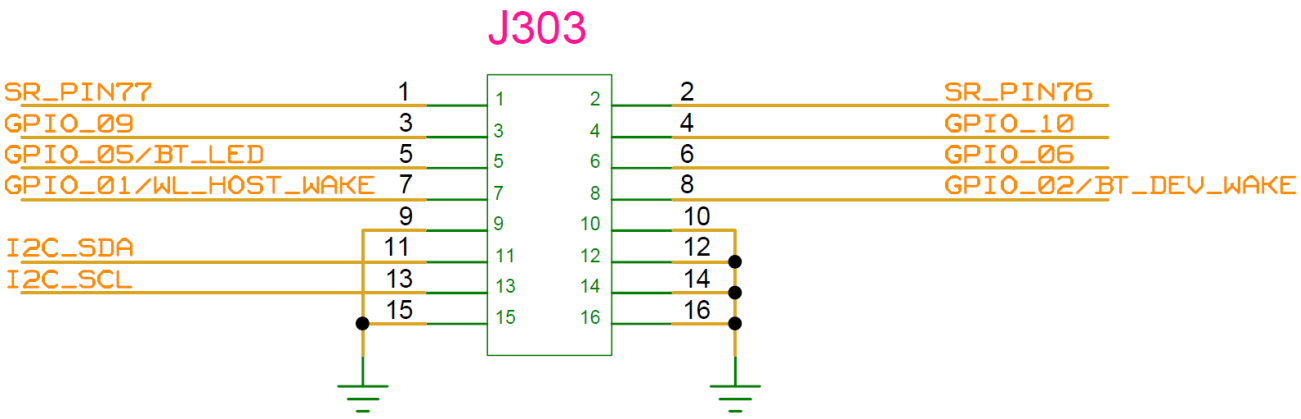


Figure 17: Connector J303

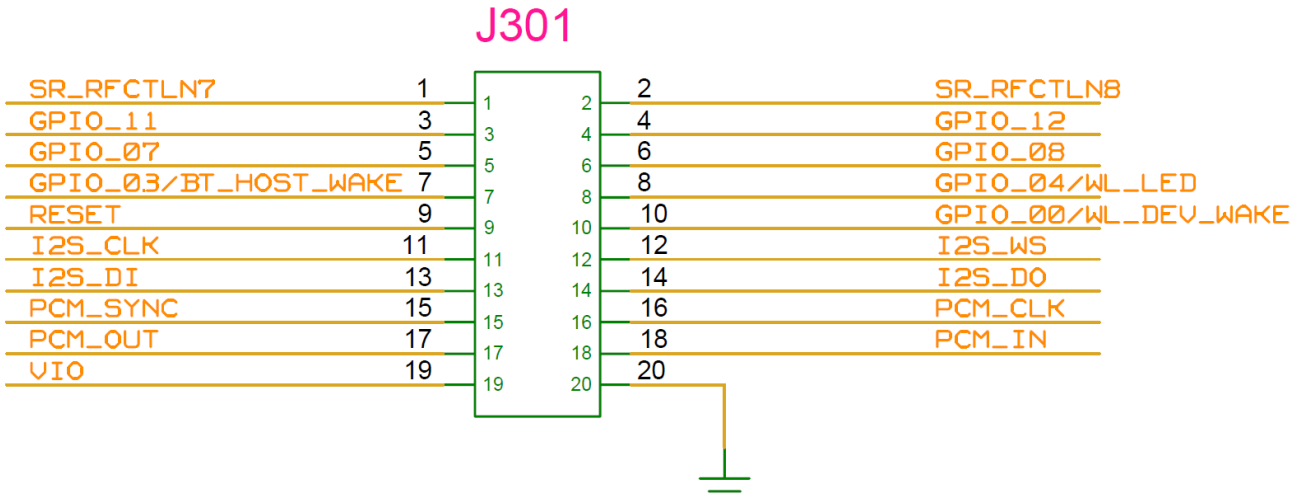


Figure 18: Connector J301

4.9 Bootstrapping

JODY-W3 supports the following host interface combinations:

- **PCIE-UART** mode: Commands and data for the Wi-Fi traffic are transferred through the PCIe bus to the module. The Bluetooth traffic uses the high-speed UART interface.
- **SDIO-UART** mode: Commands and data for the Wi-Fi traffic is transferred through the SDIO bus to the module. The Bluetooth traffic uses the high-speed UART interface.
- **SDIO-SDIO** mode: Commands and data for both the Wi-Fi and Bluetooth traffic is transferred to the module through the SDIO bus.

DIP switch SW503 is used on the EVK to define the boot up mode and the physical interfaces used for Wi-Fi and Bluetooth communication. Set each switch ON to pull the configuration signal low (GND, logic level “0”), and OFF to pull it high (logic level “1”).

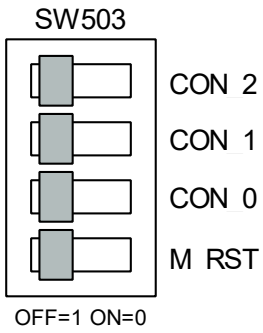


Figure 19: Boot and host interface configuration

Table 10 describes the DIP switch positions for configuring the boot mode and host interface options.

Boot mode	CON_2	CON_1	CON_0	Description
PCIE-UART	ON	OFF	OFF	WI-Fi through PCIe (J203), Bluetooth through USB-to-UART (J205) or UART (J305)
SDIO-UART	ON	ON	ON	WI-Fi through SDIO (J204), Bluetooth through USB-to-UART (J205) or UART (J305)
SDIO-SDIO	ON	ON	OFF	WI-Fi and Bluetooth through SDIO (J204)

Table 10: Boot mode selection options

☞ The UART interface for Bluetooth can be accessed either directly through J305, or through the USB type-C connector J205 via a USB-to-UART bridge. For further information about the Bluetooth UART interface, see section 4.6.

4.10 Antenna interfaces

The evaluation board includes two dual-band 2.4/5 GHz chip antennas (Pulse Electronics W3006) for Wi-Fi and Bluetooth communication. Three standard 50 Ω female SMA connectors are included to connect external antennas or measurement instruments. The antenna interfaces are selected by connecting designated u.FL connectors on the EVK with coaxial RF cables.

The module board has three u.FL connectors which connect to the antenna pins of the JODY-W3 series module. To use any of the chip antennas or SMA connectors on the EVK, connect a coaxial RF cable between the u.FL connector on the module board and u.FL connector on the carrier board, as shown in Figure 20 and Figure 21.

Table 11 describes the available radio interfaces of the modules and the default antenna interfaces which are selected on the EVK.

Product name	Module antenna pin	Function	Default antenna interface on the EVK
EVK-JODY-W374	ANT0	5GHz Wi-Fi and Bluetooth	Dual-band chip antenna ANT400
	ANT1	2.4/5 GHz Wi-Fi	Dual-band chip antenna ANT401
	ANT2	-	-
EVK-JODY-W377	ANT0	2.4/5 GHz Wi-Fi	SMA connector 2
	ANT1	2.4/5 GHz Wi-Fi	SMA connector 1
	ANT2	Bluetooth	Dual-band chip antenna ANT400

Table 11: Antenna interface configuration

☞ Connect the external antennas supplied with EVK-JODY-W377 to the selected SMA connectors. For further information about the external antennas, see also section 1.2

Default antenna configurations for EVK-JODY-W374 and EVK-JODY-W377 are shown in Figure 20 and Figure 21, respectively.

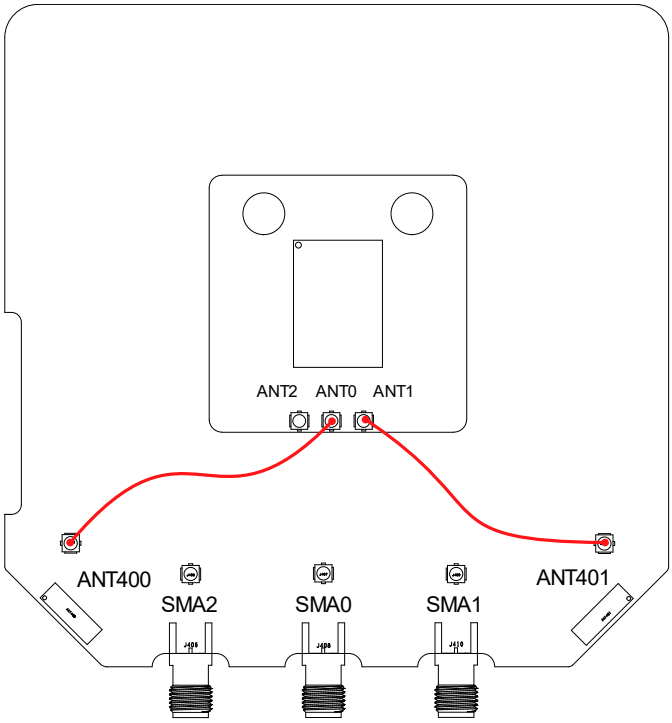


Figure 20: Default antenna configuration for EVK-JODY-W374

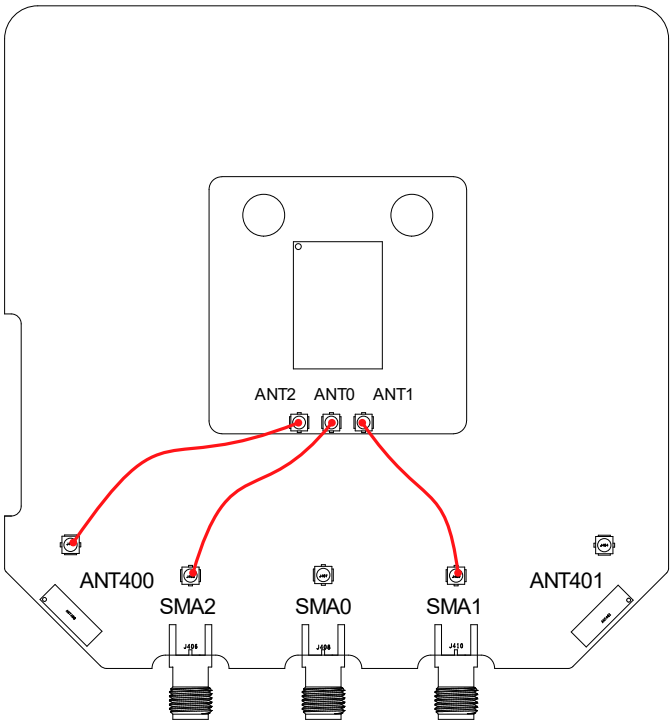


Figure 21: Default antenna configuration for EVK-JODY-W377

4.11 LEDs

Table 12 describes the function and designation of the available LEDs on the EVK-JODY-W3 evaluation board.

Function	Description	Designator	Color
VDD_EXT	External voltage supplied	D401	Green
VBAT	Main power supply (VBAT) status indication	D402	Green
VIO	VIO Supply (1.8 V or 3.3 V)	D403	Green
1V8	Aanalog power supply and SDIO (1V8)	D404	Green
VDD_3V3	Board voltage to supply for audio codecs, LEDs	D405	Green
WLAN	Wi-Fi activity signal from module GPIO	D406	Yellow
BT	Bluetooth activity signal from module GPIO	D407	Blue

Table 12: LED Description

Remove jumper J411 for accurate power measurement of the average power in low power sleep modes. With the jumper removed all LEDs will be off.

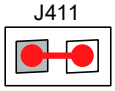


Figure 22: LED enable jumper

☞ Wi-Fi and Bluetooth activity signals from the module are not supported. WLAN and BT LEDs have no function.

4.12 Schematics

Complete schematics for the JODY-W3 evaluation board (carrier and module board) are available on request. For further information, contact your local u-blox support team.

Appendix

A Known issues

The following issues are known with the latest version of the EVK.

- The USB interface for Bluetooth does not work in the case of VIO=1.8 V, power supply over PCIe and the USB cable plugged into the host before the host PCIe initialization. To work around this issue, use external power supplies or plug the USB cable only after PCI initialization.
- When using the EVK-JODY-W3 with NXP i.MX8 series platforms, the SDIO interface cannot be used to draw the power for the module. To work around this issue, draw power through USB or external power supplies.
- Reset buttons SW500, SW501 are not working properly. This issue is to be addressed for the next board revision.

For more information about known issues, recommendations and solutions, contact your local u-blox support team.

B Glossary

Abbreviation	Definition
EVB	Evaluation board
EVK	Evaluation kit
HCI	Host controller interface
I/O	Input / output
I2S	Inter-Integrated circuit sound
LED	Light-Emitting Diode
LDO	Low-dropout regulator
LPO	Low-power oscillator
LTE	Long-Term Evolution
MAC	Medium access control
MIMO	Multiple input multiple output
MMC	Multimedia card
PC	Personal computer
PCI	Peripheral component interconnect
PCIe	Peripheral component interconnect express
PCM	Pulse-code modulation
SD	Secure digital
SDIO	Secure digital input output
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
Wi-Fi	Wireless local area network
ZIF	Zero Insertion Force

Table 13: Explanation of the abbreviations and terms used

Related documents

[1] JODY-W3 series data sheet, UBX-19010615
[2] JODY-W3 system integration manual, UBX-19011209
[3] JODY-W2 level shifter integration application note, UBX-19034257
[4] EVK-JODY-W3 schematics

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	9-Jul-2020	mzes	Initial release.
R02	2-Nov-2020	mzes	Minor editorial updates. Released for public distribution.

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