PIC16F152XX Family Product Brief

Introduction

The PIC16F152XX microcontroller family is available in 8/14/16/20/28/40/44-pin packages for cost-sensitive sensor and real-time control applications. The PIC16F152XX family's simplified feature set includes a 10-bit Analog-to-Digital Converter (ADC), Peripheral Pin Select (PPS), digital communication peripherals, timers, and waveform generators. This microcontroller family also provides memory features, such as the Memory Access Partition (MAP) to support users in data protection and bootloader applications, and a Device Information Area (DIA), which stores Fixed Voltage Reference (FVR) offset values to help improve ADC accuracy.

PIC16F152XX Family Types

Table 1. Devices included in this data sheet

Device	Program Flash Memory (bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(1)/ Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timers(2)	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	MSSP	EUSART	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F15213	3.5k	256	Y/Y	6/Y	1/2	2/2	5/2	1	1	N	1	6	Y
PIC16F15214	7k	512	Y/Y	6/Y	1/2	2/2	5/2	1	1	N	1	6	Y
PIC16F15223	3.5k	256	Y/Y	12/Y	1/2	2/2	9/2	1	1	Y	1	12	Y
PIC16F15224	7k	512	Y/Y	12/Y	1/2	2/2	9/2	1	1	Y	1	12	Y
PIC16F15225	14k	1024	Y/Y	12/Y	1/2	2/2	9/2	1	1	Y	1	12	Y
PIC16F15243	3.5k	256	Y/Y	18/Y	1/2	2/2	12/2	1	1	Y	1	18	Y
PIC16F15244	7k	512	Y/Y	18/Y	1/2	2/2	12/2	1	1	Y	1	18	Y
PIC16F15245	14k	1024	Y/Y	18/Y	1/2	2/2	12/2	1	1	Y	1	18	Y
PIC16F15254	7k	512	Y/Y	25/Y	1/2	2/2	17/2	1	1	Y	1	25	Y
PIC16F15255	14k	1024	Y/Y	25/Y	1/2	2/2	17/2	1	1	Y	1	25	Y
PIC16F15256	28k	2048	Y/Y	25/Y	1/2	2/2	17/2	1	1	Y	1	25	Y
PIC16F15274	7k	512	Y/Y	36/Y	1/2	2/2	28/2	1	1	Y	1	36	Y
PIC16F15275	14k	1024	Y/Y	36/Y	1/2	2/2	28/2	1	1	Y	1	36	Y
PIC16F15276	28k	2048	Y/Y	36/Y	1/2	2/2	28/2	1	1	Y	1	36	Y

Note:

1. Total I/O count includes one pin ($\overline{MCLR}$) that is input only.
2. Timer0 can be configured as either an 8 or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT)

Memory

- Up to 28 KB of Program Flash Memory
- Up to 2 KB of Data SRAM Memory
- Memory Access Partition (MAP): The Program Flash Memory can be partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Fixed Voltage Reference (FVR) measurement data
  - Microchip unique identifier
- Device Characteristics Area (DCI) Stores:
  - Program/erase row sizes
  - Pin count details
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Sleep:
  - Reduce device power consumption
  - Reduce system electrical noise while performing ADC conversions
- Low-Power Mode Features:
  - Sleep:
    - < 900nA typical @ 3V/25°C (WDT enabled)

    - < 600nA typical @ 3V/25°C (WDT disabled)
  - Operating Current:
    - 48μA typical @ 32 kHz, 3V/25°C
    - < 1mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- Two Capture/Compare/PWM (CCP) modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Two Pulse-Width Modulators (PWM):
  - 10-bit resolution
  - Independent pulse outputs
- One Configurable 8/16-Bit Timer (TMR0)
- One 16-Bit Timer (TMR1) with Gate Control
- One 8-Bit Timer (TMR2) with Hardware Limit Timer (HLT)
- One Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485, LIN compatible
  - Auto wake-up on Start
- One Master Synchronous Serial Port (MSSP):
  - Serial Peripheral Interface (SPI) mode
    - Slave Select Synchronization
  - Inter-Integrated Circuit (I^2C) mode
    - 7/10-bit addressing modes
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Device I/O Port Features:
  - Up to 35 I/O pins
  - 1 input-only pin
  - Individual I/O direction, open-drain, input threshold, slew rate, and weak pull-up control
  - Interrupt-on-Change (IOC) on all pins
  - One External Interrupt pin

Analog Peripherals

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 28 external input channels
  - Two internal input channels
  - Internal ADC oscillator (ADCRC)
  - Operates in Sleep
  - Selectable Auto-Conversion Trigger sources
- Fixed Voltage Reference (FVR):
  - Selectable 1.024V, 2.048V, and 4.096V output levels
  - Internally connected to ADC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):

  - Selectable frequencies up to 32 MHz
  - ±2% at calibration
- Internal 31 kHz Oscillator (LFINTOSC)
- External High-Frequency Clock Input:
  - Two External Clock (EC) power modes

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with One Breakpoint via Two Pins
- Debug Integrated On-Chip

1. Packages

Table 1-1. Packages

Device	8-Pin SOIC	8-Pin DFN	14-Pin TSSOP	14-Pin SOIC	16-Pin VQFN 3x3x0.9	20-Pin PDIP	20-Pin SSOP	20-Pin SOIC	20-Pin VQFN 3x3x0.9	28-Pin SOIC	28-Pin SSOP	28-Pin VQFN 6x6x1	40-Pin PDIP	40-Pin VQFN 5x5x0.9	44-Pin TQFP 10x10x1
PIC16F15213	•	•													
PIC16F15214	•	•													
PIC16F15223			•	•	•										
PIC16F15224			•	•	•										
PIC16F15225			•	•	•										
PIC16F15243						•	•	•	•						
PIC16F15244						•	•	•	•						
PIC16F15245						•	•	•	•						
PIC16F15254										•	•	•			
PIC16F15255										•	•	•			
PIC16F15256										•	•	•			
PIC16F15274													•	•	•
PIC16F15275													•	•	•
PIC16F15276													•	•	•

2. Pin Diagrams

Figure 2-1.

8-Pin SOIC

8-Pin DFN

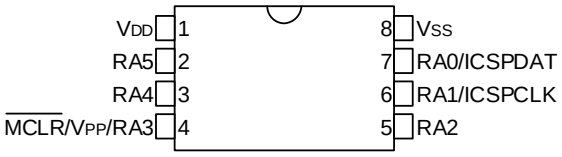


Figure 2-2.

14-Pin SOIC

14-Pin TSSOP

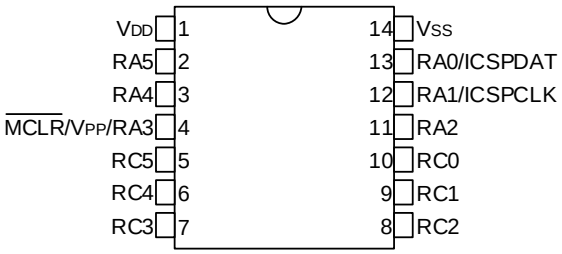
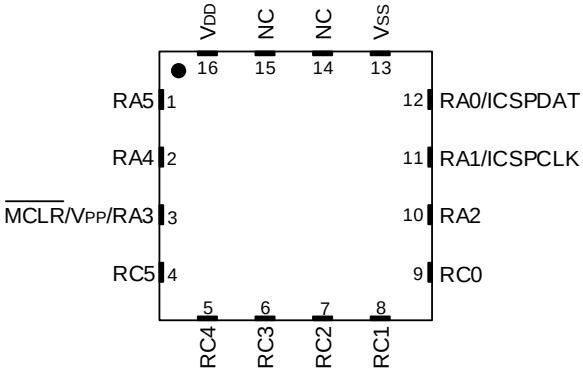


Figure 2-3.

16-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 2-4.

20-Pin PDIP

20-Pin SOIC

20-Pin SSOP

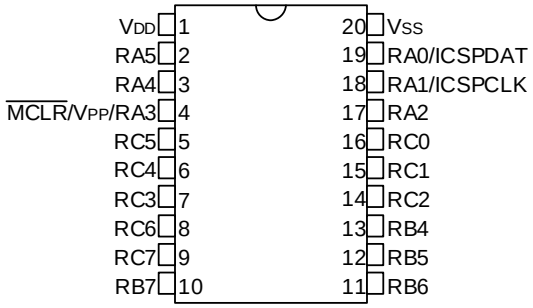
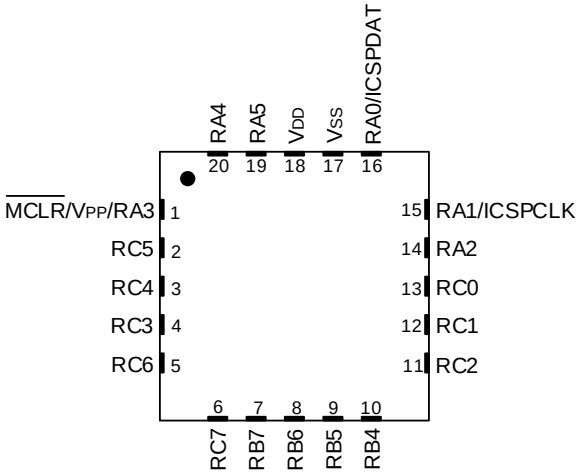


Figure 2-5.
20-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 2-6.
28-Pin SSOP

28-Pin SOIC

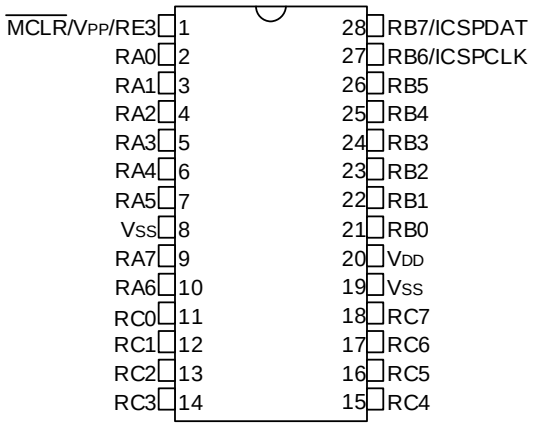
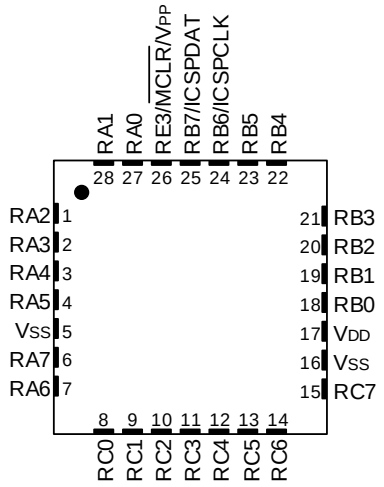


Figure 2-7.
28-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 2-8.
40-Pin PDIP

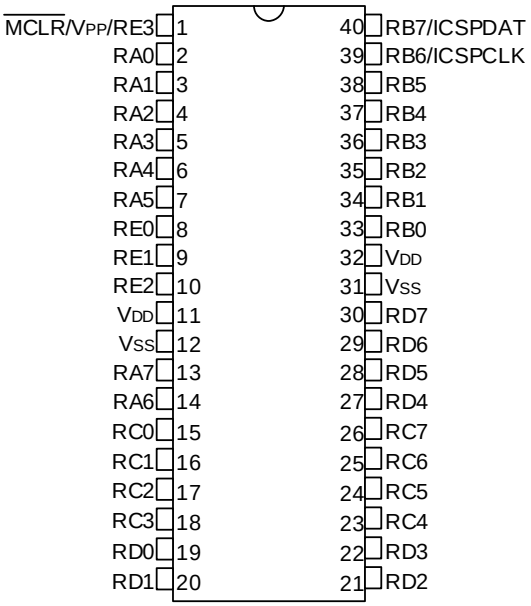
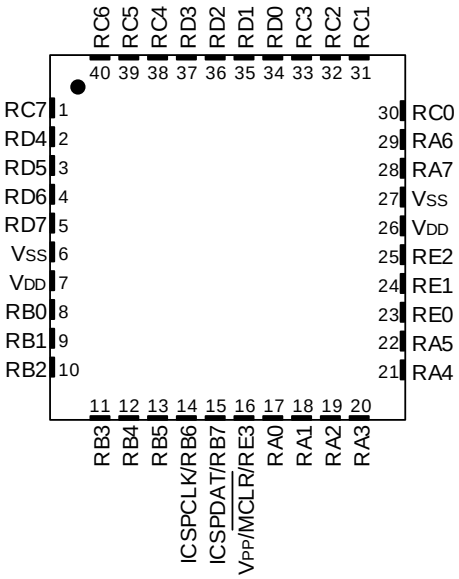


Figure 2-9.
40-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 2-10.
44-Pin TQFP

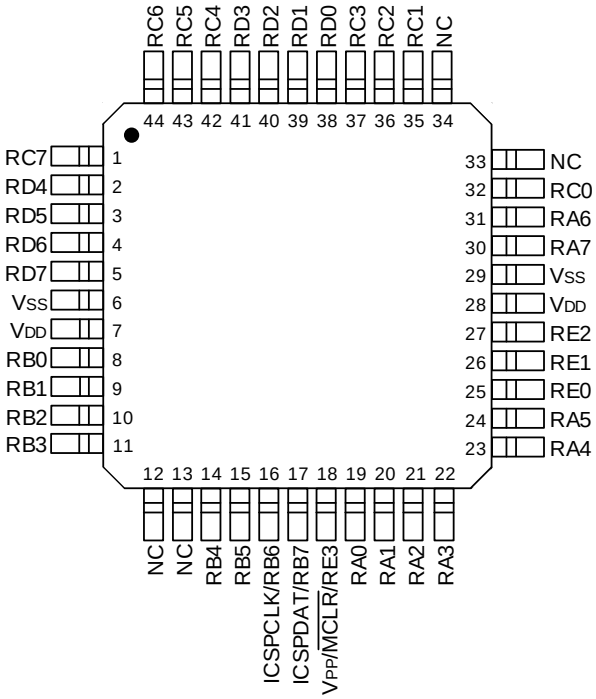


Table 3-1. 8-Pin Allocation Table

I/O	8-Pin SOIC DFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA0	7	ANA0	—	—	—	—	—	RX1(1) DT1(1,3)	IOCA0	—	ICSPDAT ICDDAT
RA1	6	ANA1	V_{REF+} (ADC)	—	—	—	SCL1(1,3) SCK1(1,3)	CK1(1,3)	IOCA1	—	ICSPCLK ICDCLK
RA2	5	ANA2	—	T0CKI(1)	—	—	SDA1(1,3) SDI1(1,3)	—	IOCA2	INT(1)	—
RA3	4	—	—	—	—	—	$\overline{SS1}$(1)	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	ANA4	—	T1G(1)	—	—	—	—	IOCA4	—	CLKOUT
RA5	2	ANA5 ADACT(1)	—	T1CKI(1) T2IN(1)	CCP1(1) CCP2(1)	—	—	—	IOCA5	—	CLKIN
V_{DD}	1	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	SCL1 SCK1 SDA1 SDO1	TX1 DT1 CK1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.

Table 3-2. 14/16-Pin Allocation Table

I/O	14-Pin SOIC TSSOP	16-Pin VQFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA0	13	12	ANA0	—	—	—	—	—	—	IOCA0	—	ICSPDAT ICDDAT
RA1	12	11	ANA1	V_{REF+} (ADC)	—	—	—	—	—	IOCA1	—	ICSPCLK ICDCLK
RA2	11	10	ANA2	—	T0CKI(1)	—	—	—	—	IOCA2	INT(1)	—
RA3	4	3	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	2	ANA4	—	T1G(1)	—	—	—	—	IOCA4	—	CLKOUT
RA5	2	1	ANA5	—	T1CKI(1) T2IN(1)	—	—	—	—	IOCA5	—	CLKIN
RC0	10	9	—	—	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCC0	—	—
RC1	9	8	—	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCC1	—	—
RC2	8	7	ANC2 ADACT(1)	—	—	—	—	—	—	IOCC2	—	—
RC3	7	6	ANC3	—	—	CCP2(1)	—	$\overline{SS1}$(1)	—	IOCC3	—	—
RC4	6	5	ANC4	—	—	—	—	—	CK1(1,3)	IOCC4	—	—
RC5	5	4	ANC5	—	—	CCP1(1)	—	—	RX1(1) DT1(1,3)	IOCC5	—	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	SCL1 SCK1 SDA1 SDO1	TX1 DT1 CK1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

Table 3-3. 20-Pin Allocation Table

I/O	20-Pin PDIP SSOP SOIC	20-Pin VQFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA0	19	16	ANA0	—	—	—	—	—	—	IOCA0	—	ICSPDAT ICDDAT
RA1	18	15	ANA1	V_{REF+} (ADC)	—	—	—	—	—	IOCA1	—	ICSPCLK ICDCLK
RA2	17	14	ANA2	—	T0CKI(1)	—	—	—	—	IOCA2	INT(1)	—
RA3	4	1	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	T1G(1)	—	—	—	—	IOCA4	—	CLKOUT

.....continued

I/O	20-Pin PDIP SSOP SOIC	20-Pin VQFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA5	2	19	ANA5	—	T1CKI(1) T2IN(1)	—	—	—	—	IOCA5	—	CLKIN
RB4	13	10	—	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCB4	—	—
RB5	12	9	ANB5	—	—	—	—	—	RX1(1) DT1(1,3)	IOCB5	—	—
RB6	11	8	ANB6	—	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCB6	—	—
RB7	10	7	ANB7	—	—	—	—	—	CK1(1,3)	IOCB7	—	—
RC0	16	13	—	—	—	—	—	—	—	IOCC0	—	—
RC1	15	12	—	—	—	—	—	—	—	IOCC1	—	—
RC2	14	11	ANC2 ADACT(1)	—	—	—	—	—	—	IOCC2	—	—
RC3	7	4	ANC3	—	—	CCP2(1)	—	—	—	IOCC3	—	—
RC4	6	3	ANC4	—	—	—	—	—	—	IOCC4	—	—
RC5	5	2	ANC5	—	—	CCP1(1)	—	—	—	IOCC5	—	—
RC6	8	5	—	—	—	—	—	$\overline{SS1}$(1)	—	IOCC6	—	—
RC7	9	6	—	—	—	—	—	—	—	IOCC7	—	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	SCL1 SCK1 SDA1 SDO1	TX1 DT1 CK1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

Table 3-4. 28-Pin Allocation Table

I/O	28-Pin SOIC SSOP	28-Pin VQFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA0	2	27	ANA0	—	—	—	—	—	—	IOCA0	—	—
RA1	3	28	ANA1	—	—	—	—	—	—	IOCA1	—	—
RA2	4	1	ANA2	—	—	—	—	—	—	IOCA2	—	—
RA3	5	2	ANA3	V_{REF}+ (ADC)	—	—	—	—	—	IOCA3	—	—
RA4	6	3	—	—	T0CKI(1)	—	—	—	—	IOCA4	—	—
RA5	7	4	ANA5	—	—	—	—	$\overline{SS1}$(1)	—	IOCA5	—	—
RA6	10	7	—	—	—	—	—	—	—	IOCA6	—	CLKOUT
RA7	9	6	—	—	—	—	—	—	—	IOCA7	—	CLKIN

.....continued

I/O	28-Pin SOIC SSOP	28-Pin VQFN	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RB0	21	18	ANB0	—	—	—	—	—	—	IOCB0	INT(1)	—
RB1	22	19	ANB1	—	—	—	—	—	—	IOCB1	—	—
RB2	23	20	ANB2	—	—	—	—	—	—	IOCB2	—	—
RB3	24	21	ANB3	—	—	—	—	—	—	IOCB3	—	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	—	—	—	IOCB4	—	—
RB5	26	23	ANB5	—	T1G(1)	—	—	—	—	IOCB5	—	—
RB6	27	24	—	—	—	—	—	—	—	IOCB6	—	ICSPCLK ICDCLK
RB7	28	25	—	—	—	—	—	—	—	IOCB7	—	ICSPDAT ICDDAT
RC0	11	8	—	—	T1CKI(1)	—	—	—	—	IOCC0	—	—
RC1	12	9	—	—	—	CCP2(1)	—	—	—	IOCC1	—	—
RC2	13	10	ANC2	—	—	CCP1(1)	—	—	—	IOCC2	—	—
RC3	14	11	ANC3	—	T2IN(1)	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCC3	—	—
RC4	15	12	ANC4	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCC4	—	—
RC5	16	13	ANC5	—	—	—	—	—	—	IOCC5	—	—
RC6	17	14	ANC6	—	—	—	—	—	CK1(1,3)	IOCC6	—	—
RC7	18	15	ANC7	—	—	—	—	—	RX1(1) DT1(1,3)	IOCC7	—	—
RE3	1	26	—	—	—	—	—	—	—	IOCE3	—	$\overline{MCLR}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8 19	5 16	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	SCL1 SCK1 SDA1 SDO1	TX1 DT1 CK1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the PPS input table in the device data sheet for details on which PORT pins may be used for this signal.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

Table 3-5. 40/44-Pin Allocation Table

I/O	40-Pin PDIP	40-Pin VQFN	44-Pin TQFP	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA0	2	17	19	ANA0	—	—	—	—	—	—	IOCA0	—	—
RA1	3	18	20	ANA1	—	—	—	—	—	—	IOCA1	—	—
RA2	4	19	21	ANA2	—	—	—	—	—	—	IOCA2	—	—

.....continued

I/O	40-Pin PDIP	40-Pin VQFN	44-Pin TQFP	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
RA3	5	20	22	ANA3	V_{REF+} (ADC)	—	—	—	—	—	IOCA3	—	—
RA4	6	21	23	—	—	T0CKI(1)	—	—	—	—	IOCA4	—	—
RA5	7	22	24	ANA5	—	—	—	—	$\overline{SS1}$(1)	—	IOCA5	—	—
RA6	14	29	31	—	—	—	—	—	—	—	IOCA6	—	CLKOUT
RA7	13	28	30	—	—	—	—	—	—	—	IOCA7	—	CLKIN
RB0	33	8	8	ANB0	—	—	—	—	—	—	IOCB0	INT(1)	—
RB1	34	9	9	ANB1	—	—	—	—	—	—	IOCB1	—	—
RB2	35	10	10	ANB2	—	—	—	—	—	—	IOCB2	—	—
RB3	36	11	11	ANB3	—	—	—	—	—	—	IOCB3	—	—
RB4	37	12	14	ANB4 ADACT(1)	—	—	—	—	—	—	IOCB4	—	—
RB5	38	13	15	ANB5	—	T1G(1)	—	—	—	—	IOCB5	—	—
RB6	39	14	16	—	—	—	—	—	—	—	IOCB6	—	ICSPCLK ICDCLK
RB7	40	15	17	—	—	—	—	—	—	—	IOCB7	—	ICSPDAT ICDDAT
RC0	15	30	32	—	—	T1CKI(1)	—	—	—	—	IOCC0	—	—
RC1	16	31	35	—	—	—	CCP2(1)	—	—	—	IOCC1	—	—
RC2	17	32	36	ANC2	—	—	CCP1(1)	—	—	—	IOCC2	—	—
RC3	18	33	37	ANC3	—	T2IN(1)	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCC3	—	—
RC4	23	38	42	ANC4	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCC4	—	—
RC5	24	39	43	ANC5	—	—	—	—	—	—	IOCC5	—	—
RC6	25	40	44	ANC6	—	—	—	—	—	CK1(1,3)	IOCC6	—	—
RC7	26	1	1	ANC7	—	—	—	—	—	RX1(1) DT1(1,3)	IOCC7	—	—
RD0	19	34	38	AND0	—	—	—	—	—	—	IOCD0	—	—
RD1	20	35	39	AND1	—	—	—	—	—	—	IOCD1	—	—
RD2	21	36	40	AND2	—	—	—	—	—	—	IOCD2	—	—
RD3	22	37	41	AND3	—	—	—	—	—	—	IOCD3	—	—
RD4	27	2	2	AND4	—	—	—	—	—	—	IOCD4	—	—
RD5	28	3	3	AND5	—	—	—	—	—	—	IOCD5	—	—
RD6	29	4	4	AND6	—	—	—	—	—	—	IOCD6	—	—
RD7	30	5	5	AND7	—	—	—	—	—	—	IOCD7	—	—
RE0	8	23	25	ANE0	—	—	—	—	—	—	IOCE0	—	—
RE1	9	24	26	ANE1	—	—	—	—	—	—	IOCE1	—	—
RE2	10	25	27	ANE2	—	—	—	—	—	—	IOCE2	—	—
RE3	1	16	18	—	—	—	—	—	—	—	IOCE3	—	$\overline{MCLR}$ V_{PP}
V_{DD}	11 32	7 26	7 28	—	—	—	—	—	—	—	—	—	V_{DD}

.....continued

I/O	40-Pin PDIP	40-Pin VQFN	44-Pin TQFP	ADC	Reference	Timers	CCP	10-Bit PWM	MSSP	EUSART	IOC	Interrupt	Basic
V_{SS}	12 31	6 27	6 29	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—		—	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	SCL1 SCK1 SDA1 SDO1	TX1 DT1 CK1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the PPS input table in the device data sheet for details on which PORT pins may be used for this signal.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

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ISBN: 978-1-5224-5304-8

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