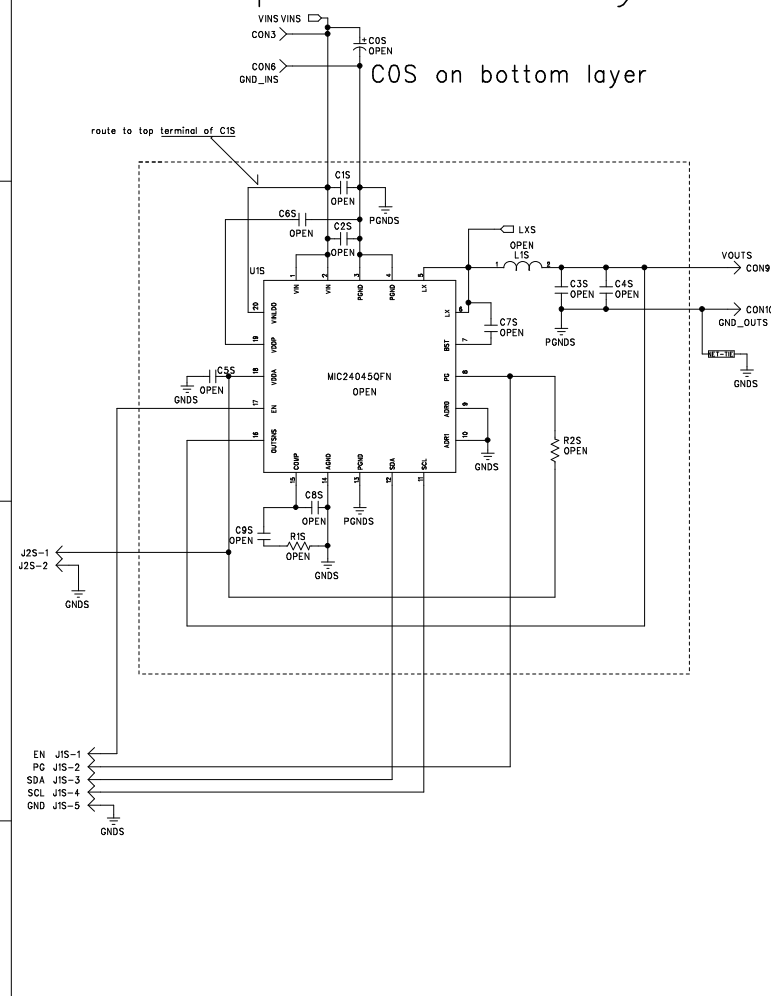
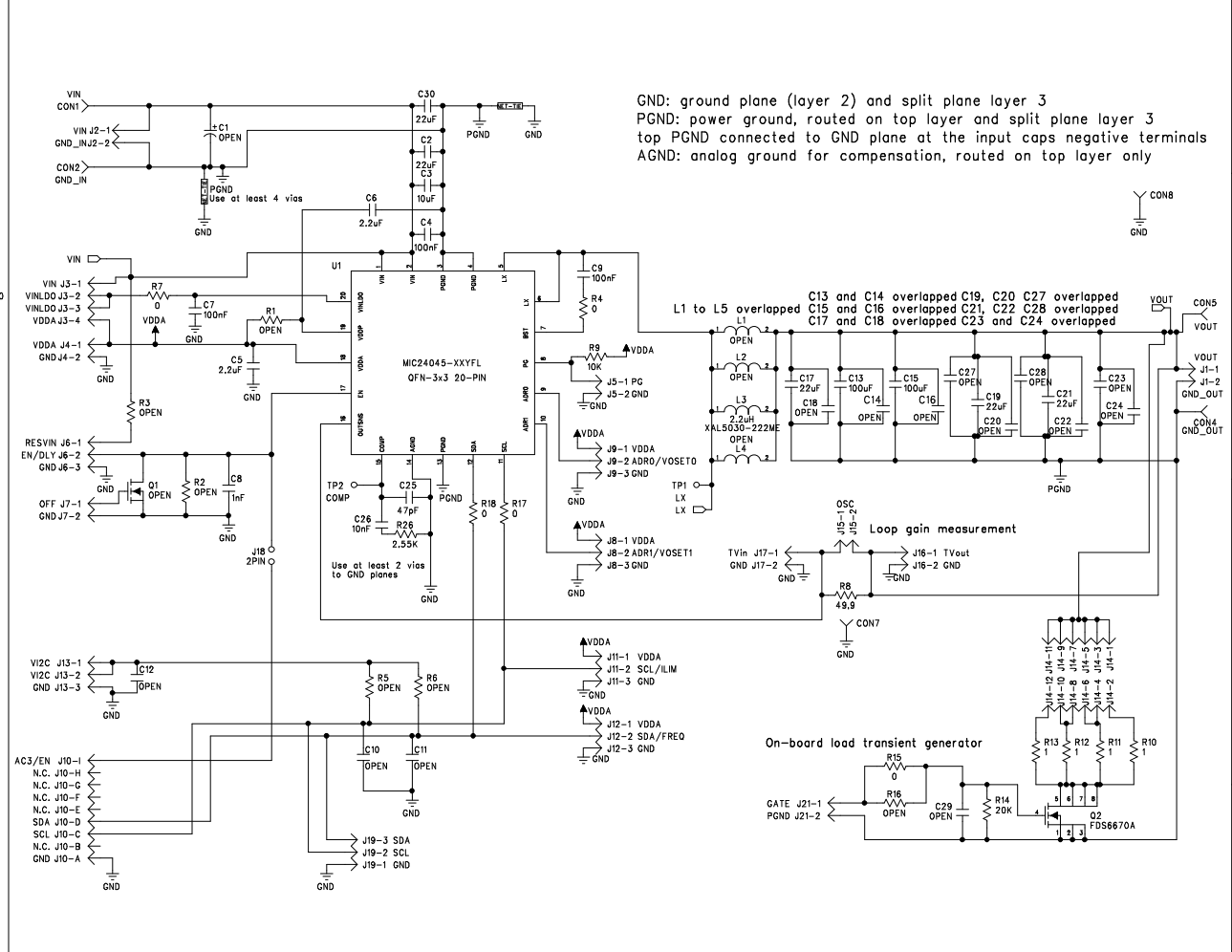


# Size-optimized layout



# Functional Eval Board Section



REVISION RECORD			
REV	DESCRIPTION	APPROVAL	DATE
01	PRELIMINARY		00/00/00
A	ORIGINAL RELEASE		00/00/00

GND: ground plane (layer 2) and split plane layer 3  
 PGND: power ground, routed on top layer and split plane layer 3  
 top PGND connected to GND plane at the input caps negative terminals  
 AGND: analog ground for compensation, routed on top layer only

L1 to L5 overlapped  
 C13 and C14 overlapped  
 C15 and C16 overlapped  
 C17 and C18 overlapped  
 C19, C20, C27 overlapped  
 C21, C22, C28 overlapped  
 C23 and C24 overlapped

Loop gain measurement

On-board load transient generator

APPROVALS	DATE	MICREL SEMICONDUCTOR	2180 FORTUNE DR. SAN JOSE, CA 95131 (408) 944-0800
ENGINEER	5/6/16	EM24045CP-D1X-SCHB	
DES WGR		MIC24045-XXYFL	EV B
ENG WGR		DOCUMENT NUMBER	REV
OTHER		EM24045CP-D1X-SCHB	B