User Guide

Pinnacle™ 100 Development Kit
Part # 453-00010-K1 and 453-00011-K1

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	22 Jan 2020	Initial Version	Mike Richter	Jonathan Kaye

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CONTENTS

1 OVERVIEW

The Laird Connectivity Pinnacle™ 100 development kit provides a platform for rapid BLE and cellular connectivity prototyping, providing multiple options for the development of Cellular IoT, Bluetooth Low Energy (BLE) plus Near Field Communication (NFC) applications. This document describes the development board hardware, highlighting the setup and interfaces available to maximize user flexibility in developing these applications.

This document is applicable to the version of development board which has PCB silk screen text 750-00251-R4.0.

2 LAIRD CONNECTIVITY PINNACLE™ 100 DEVELOPMENT KIT PART NUMBERS

Part Number	Product Description
453-00010-K1	Development Kit for the 453-00010 modem – Integrated antenna
453-00011-K1	Development Kit for the 453-00011 modem – 3 U.FL, external antenna

Applicable to the following Pinnacle™ 100 modem part numbers:

Part Number	Product Description
453-00010	Pinnacle™ 100 Modem, U.FL and integrated antenna
453-00011	Pinnacle™ 100 Modem, 3 U.FL – external antenna

3 PACKAGE CONTENTS

All kits contain the following items:

Development Board	The development board (with the Pinnacle™ 100 Modem) contains CON1 which is used to attach the Pinnacle™ 100 modem and is held in place by screws.
Hardware	Two M2 Screws to secure modem, Four Plastic Standoffs and nuts
Power Options	▪ USB cable – Type A to micro type B ▪ DC power jack for external power supply (12 VDC max) ▪ AA or AAA battery packs – Not included
SIM Card	US: customer can choose between an AT&T or Verizon SIM card to activate on the cellular network. Europe: MVNO SIM card to activate on the cellular network.
External Dual Band LTE Revie Flex antenna	Supplied with development kit part # 453-00011-K1 only. External antenna, 687-875 MHz 1.9 dBi and 1710-2500 MHz 3.7 dBi Revie Flex (Laird Connectivity part # EFF6925A3S-15MHF1) with integral RF coaxial cable with 153 mm length and IPEX MHF1 (U.FL) RF connector
External 2.4 GHz BLE FlexPIFA antenna	Supplied with development kit part # 453-00011-K1 only. External antenna, 2 dBi, FlexPIFA (Laird Connectivity part #001-0014) with integral RF coaxial cable with 100 mm length and IPEX MHF1 compatible RF connector.
External NFC antenna	Laird Connectivity NFC flexi-PCB antenna – Part # 0600-00061
BME280 BLE Sensor and Battery	BME280 BL654 Sensor Tag and CR2477 battery

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4 PINNACLE™ 100 DEVELOPMENT KIT – MAIN DEVELOPMENT BOARD

This section describes the Pinnacle™ 100 development board hardware. The Pinnacle™ 100 development board is delivered with the Pinnacle™ 100 series modem loaded with Zephyr Out of Box (OOB) example code.

The Pinnacle™ 100 development board is a universal development tool that highlights the capabilities of the Pinnacle™ 100 modem. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers several header connectors that help isolate on-board sensors and UART from the Pinnacle™ 100 modem to create different configurations. This allows you to test different operating scenarios.

The board allows the Pinnacle™ 100 series modem to physically connect to a PC via the supplied USB cable for development purposes. The development board provides USB-to-Virtual COM port conversion through a FTDI chip – part number FT232R. Any Windows PC (XP or later) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from http://www.ftdichip.com/Drivers/VCP.htm

4.1 Key Features

The Pinnacle™ 100 development board has the following features:

- M.2, KEY E, PCI connector to connect a Pinnacle™ 100 series modem into the development board
- The following power supply options for powering the development board:
  - USB (micro-USB, type B)
  - External DC supply (4.4-12V) – supplied. Center positive barrel connector or header for bench supply.
  - (4) AA batteries – not supplied. Assume Lithium Iron Disulfide (4.4 – 7.2V)
  - (2) AA batteries – not supplied. Assume Lithium Iron Disulfide (2.2 – 3.6V)
- When powering the DVK with USB, Ext DC, or 4 AA, a DC-DC converter is used to supply the DVK with 3.7V. The DVK also includes regulated 1.8V and a regulated 3.3V.
- When powering with 2AA, the DC-DC converter is bypassed, as well as the regulated 3.3V
- Placing a coin-cell (CR2032) in J13, provides a backup power supply to HL7800 RTC. (Not currently supported)
- USB FTDI (J30) to UART bridge (FTDI chip)
- Pinnacle™ 100 UART can be interfaced to:
  - USB FTDI using the USB-UART bridge (FTDI chip)
  - An external UART using J12.
- Pinnacle™ 100 modem only current measuring option:
  - J4 Pin header (ammeter)
- IO break-out 2.54-mm pitch pin header connectors that bring out all interfaces of the Pinnacle™ 100 modem – UART, SPI, I2C, SIO [DIO or AIN (ADCs)], NFC – and allows for plugging in external modules/sensors.
- DIP switches on all Pinnacle™ modem IO lines running to peripheral devices on the development board to allow disconnection.
- On-board Bosch Sensortec BME680 environmental sensor
- Four buttons and four LEDs for user interaction
- One reset button
- NFC antenna connector on-board development board for use with supplied flexi-PCB NFC antenna
- Debug and program NRF software using both an internal and an external serial wire debug (SWD)or trace interface
- GPS antenna
- *Optional* footprint for Microchip ATECC608A-SSHDA authentication IC (not populated)
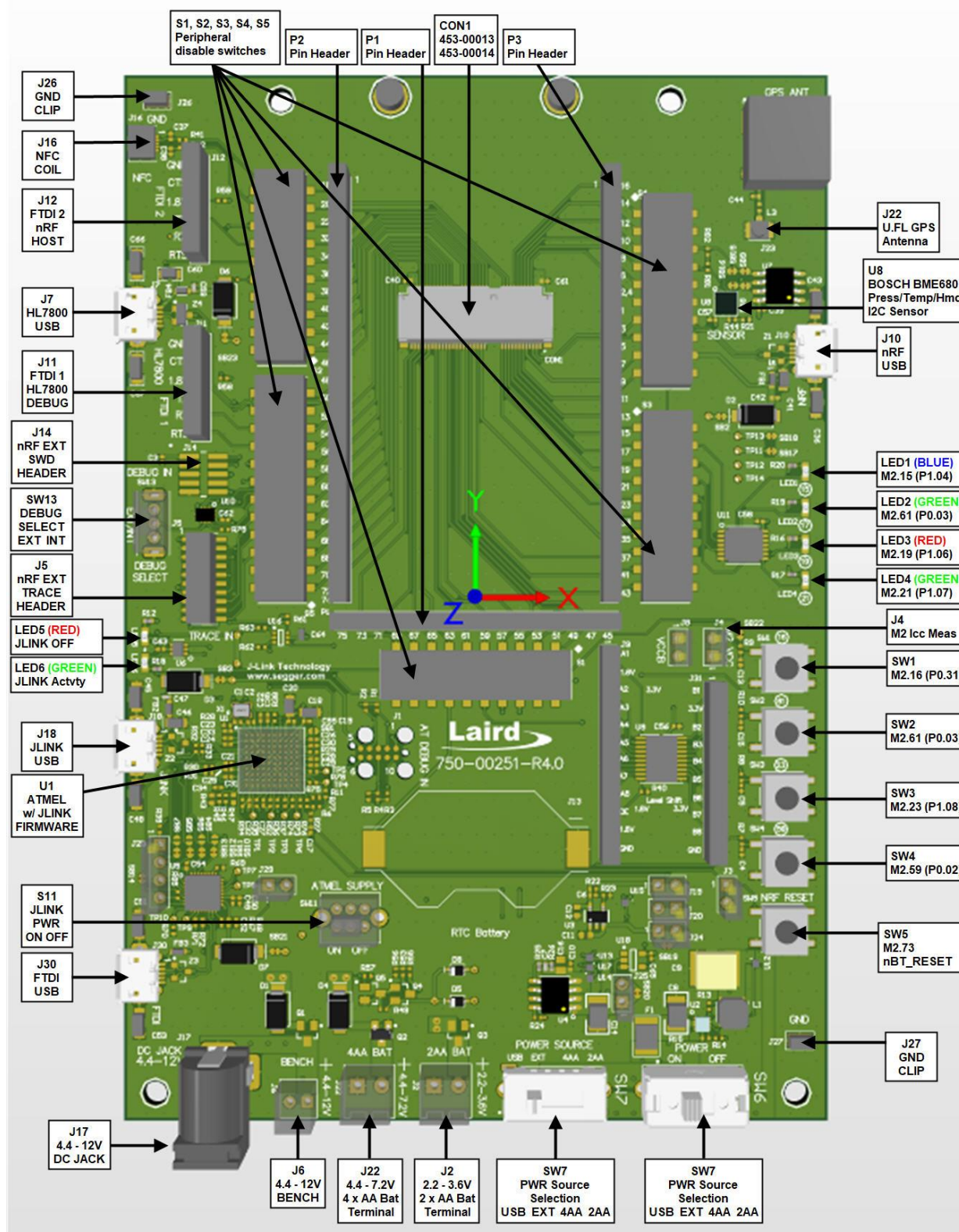- *Optional Spare Level Shifter*

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5 UNDERSTANDING THE DEVELOPMENT BOARD

Figure 1: Dev board contents and locations

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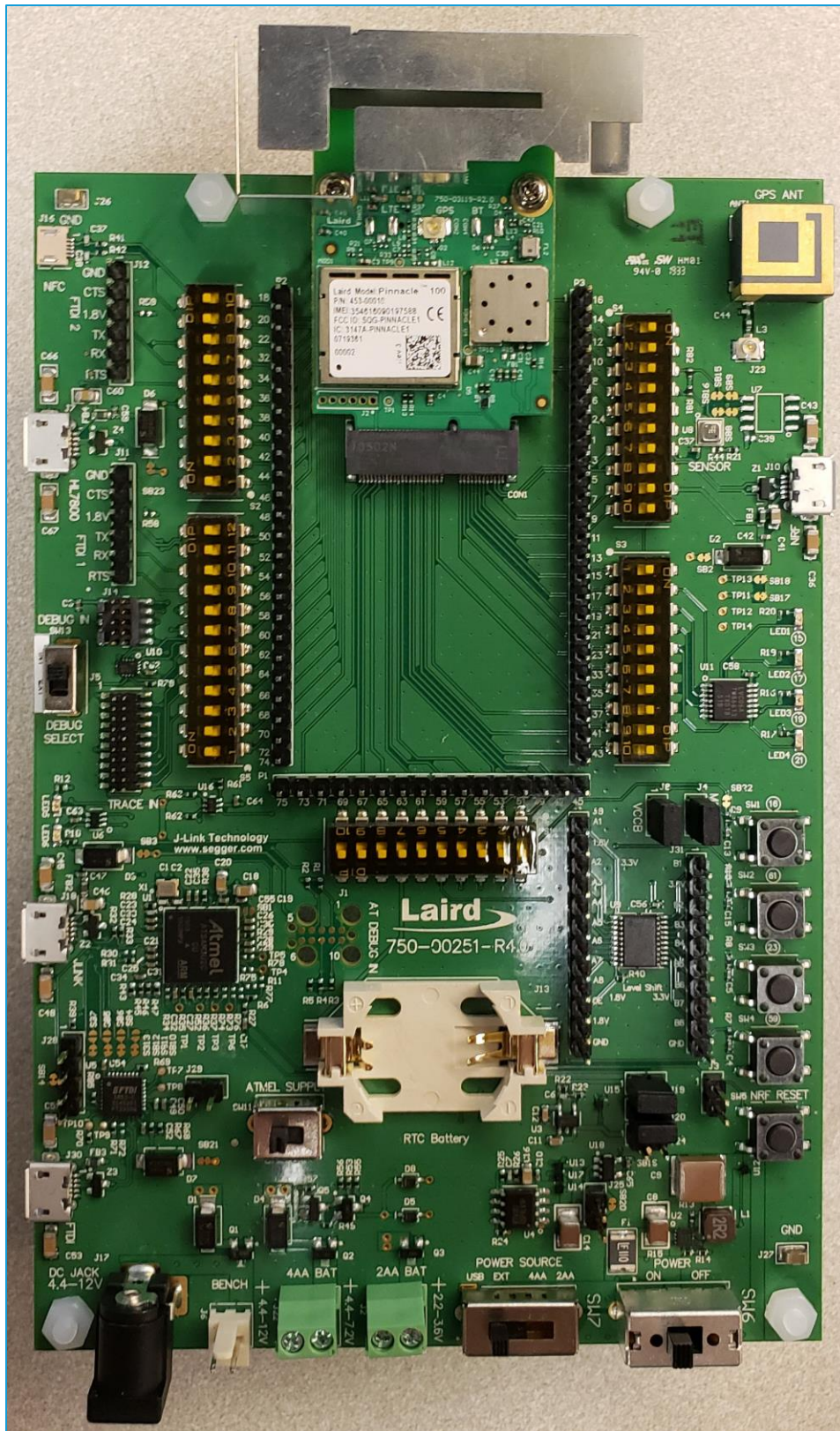
Figure 2: Development board 453-00010-K1 (fitted with 453-00010 Pinnacle™ 100 modem with integrated antenna)

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5.1 Pinnacle™ 100 Default Configuration and Jumper Settings

Note: To ensure correct out-of-the-box configuration, the Pinnacle™ 100 development board switches must be configured as shown in Figure 3. The default recommend power connection is USB with FTDI USB, J30 connected.

Figure 3: Default Pinnacle™ 100 development board 453-00010-K1 jumper and switch settings (image for 453-00010)

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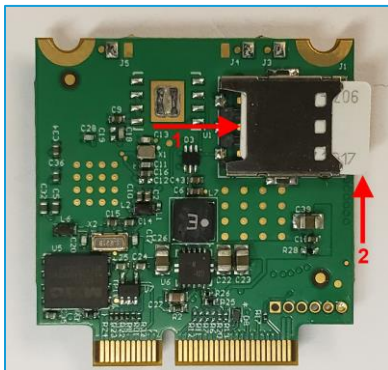**Europe**: +44-1628-858-940
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5.2 SIM Card Insertion

A nano SIM card must be inserted prior to insertion into CON1 (see Figure 4).

Figure 4: Insertion of nano SIM into a Pinnacle^{TM} 100 modem (image of 453-00010)

To remove the nano SIM, start by pushing the SIM from the back to the metal edge (arrow 1 shown in Figure 5), grab the edge of the SIM card (arrow 2), and pull out.

Figure 5: Removing nano SIM from Pinnacle^{TM} 100 modem

5.3 Modem Attachment

5.3.1   453-00011 Modems

Place the modem into CON1 and use the two provided M2 screws to thread into the standoffs to hold the modem down.

Both screws must be securely tightened to the modem and standoffs for proper modem operation. The standoffs provide additional RF grounding for the modem. Loose screws can affect antenna performance. Figure 6 shows the process of attaching a 453-00011 modem to a DVK.

Figure 6: Attaching a 453-00011 Pinnacle^{TM} 100 modem to a DVK

5.3.2 453-00010 Modems

Figure 7 shows the process of attaching a 453-00010 modem to a DVK. Recommend putting screws in the PCB holes before inserting the modem into CON1.

Figure 7: Attaching a 453-00010 Pinnacle^{TM} 100 modem to a DVK

5.4 U.FL Antenna Attachment – DVK 453-00011-K1 Only

The DVK comes with a Revie Flex EFF6925A3S-15MHF1 antenna for the LTE radio and a FlexPIFA 001-0014 for the BLE radio. Figure 8 shows the Revie Flex and FlexPIFA antennas attached to a 453-00011 modem. Both antennas must be placed on plastic for proper operation
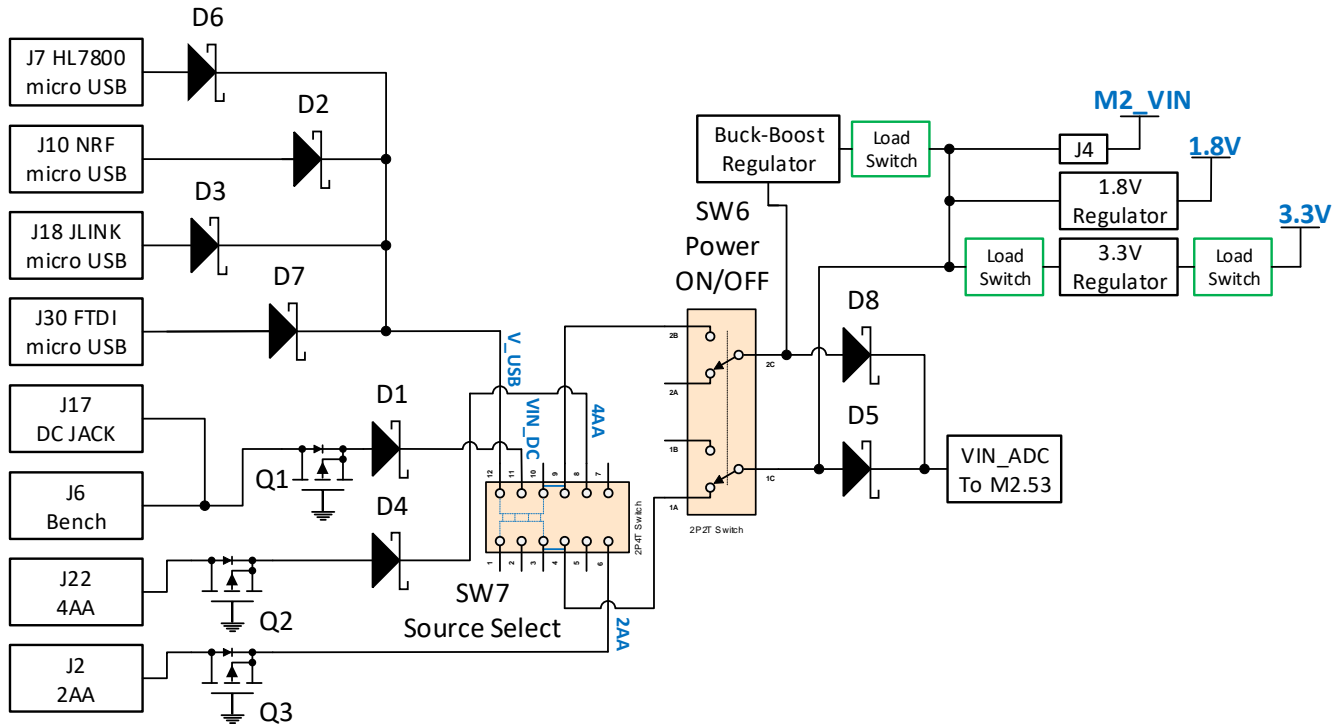

Figure 8: External antenna attachment for 453-00011 Pinnacle^{TM} 100 modem

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6 DVK FUNCTIONAL BLOCKS

6.1 Power Supply

Figure 9 shows the Pinnacle™ 100 development board power supply block diagram.

Figure 9: Pinnacle™ 100 development kit power supply diagram

There are multiple options for powering the development board:

- FTDI USB port, J30, micro-B connector – If it requires the FTDI UART to USB path (**DEFAULT)**
- JLINK USB port, J18, micro-B connector – If it requires the SWD to USB path*
- HL7800 USB port, J7, micro-B connector – If it requires the HL7800 to USB path**
- NRF USB port, J10, micro-B connector – If it requires the NRF to USB (Pinnacle™ 100) path
- An external DC supply (4.4V-12V), connected to either the DC Plug, J17, or the Bench connector, J6
- 4 x AA batteries – Four AA Energizer Lithium (4.4-7.2V) batteries connected to terminal block, J22
- 2 x AA batteries – Two AA Energizer Lithium (2.2-3.6V) batteries connected to terminal block, J2

Note: * – Connect USB cables to both J18 and J30

** – Connect USB cables to both J7 and J10

Recommend using a 1A or above for USB port connections

VIN_ADC is intended for 2AA or 4AA battery measurement and is not intended for ext DC voltages above 7.2V.

The power sources are first selected by setting SW7 (Source Select switch) to the desired power option (includes USB, external DC supply, 4AA batteries, and 2AA batteries). The selected power option is then fed into SW6, which is the ON/OFF switch for the DVK. For all power option, except 2AA, the output of SW6 is fed into a Buck-Boost regulator that feeds both a 1.8V and 3.3V linear regulator. The output of the Buck-Boost Regulator is also fed to the Pinnacle™ 100 modem VIN pins through J4 which allows for modem current measurements.

The Power supply circuit uses load switches to isolate nets from each other, this allows the Buck-Boost Regulator to be bypassed when connecting 2AA batteries and to directly power the modem, the 1.8V regulator is enabled for IO support.

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6.2 NRF Reset Button

The development board has an NRF reset button (SW5) which is routed to a AND gate along with FTDI Reset and External SWD Reset. The signal is routed through S1 DIP switch #10 with the net name nBT_RESET. The nBT_RESET signal is active low when SW5 is pushed. The placement of the NRF reset button is shown in Figure 10. The DIP switch and the AND gate are shown in Figure 11.
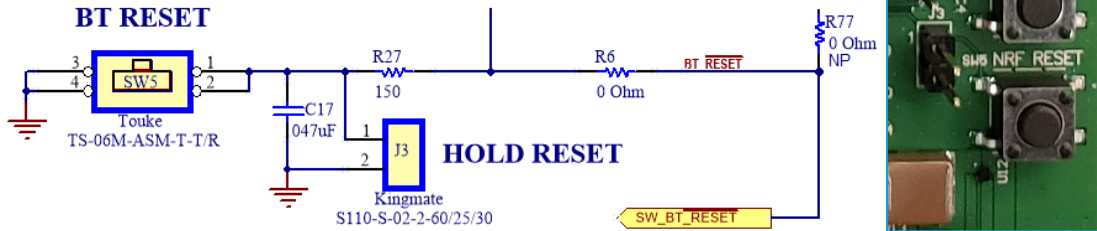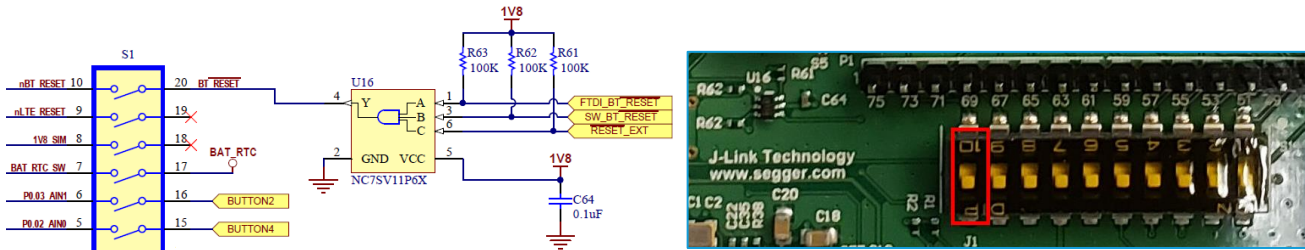

Figure 10: Pinnacle™ 100 development kit reset button

Figure 11: NRF reset schematic and routing through DIP switch S1.10 & AND gate

6.3 SWD Interface

The development board provides two options for connecting to the modem's SWD interface, the signals SWDIO, SWDCLK, and SWO, are switched by U10 based on the position on SW13 **DEBUG SELECT**:

- External header (J14) allows an external SWD debugger/programmer to be connected to the modem. The **DEBUG SELECT** (SW13) must be set to **EXTERNAL**.
- The internal SWD circuitry can also be connected to the modem. The DEBUG SELECT must be set to INTERNAL. The ATMEL SUPPLY switch, SW13, must be set to ON. USB cables must be plugged into J18 (JLINK) and J30 (FTDI), shown in Figure 13.
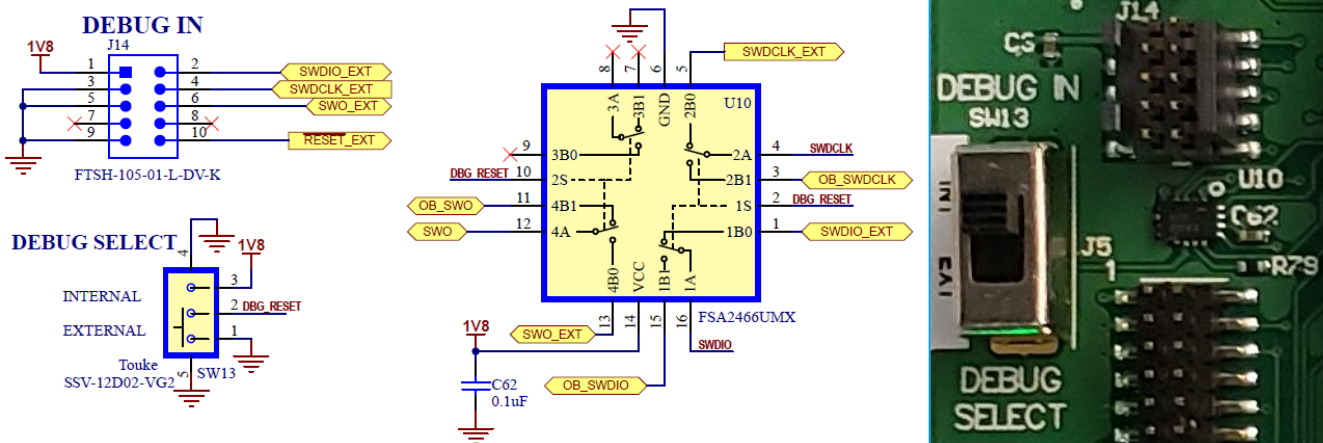
JLINK USB, FTDI USB, and ATMEL SUPPLY switch

Figure 12: SWD external header, debug select switch and analog switch U10

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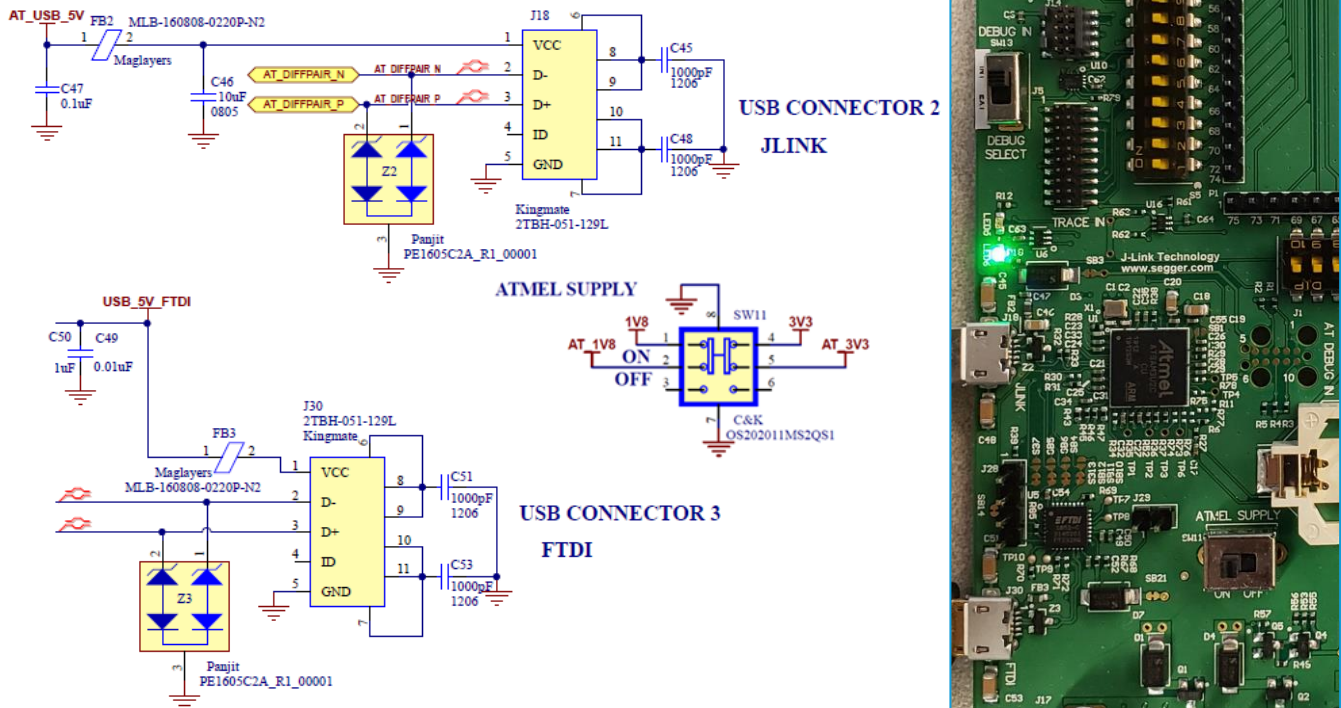**Hong Kong**: +852 2923 0610

Figure 13: JLINK USB, FTDI USB, and ATMEL SUPPLY switch

Note: We recommend that you use SWD (two-wire interface) to handle future Pinnacle™ 100 modem firmware upgrades. You MUST wire out the SWD (two-wire interface) on your host design (Four lines required: SWDIO [1.8V Logic], SWDCLK [1.8V Logic], GND, and VIN (2.2-5.5)].

M2.60 (P1.00) can be used as SWO (Serial Wire Output) and is not necessary for programming Pinnacle™ 100 over the SWD interface.

M2.73, nReset_BLE, is not necessary for programming Pinnacle™ 100 over the SWD interface.

6.4 NRF and HL7800 USB

The NRF has a direct USB connection, J10 (NRF USB). The HL7800 also has a direct USB connection, J7 (HL7800 USB). Figure 14, shows both USB connectors and J10 must be connected when using J7, to provide 5V to the modem pin M2.9.
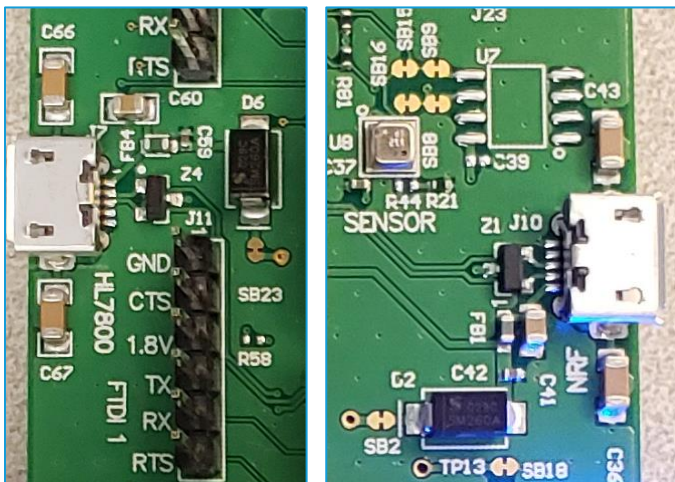

Figure 14: NRF and HL7800 USB

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6.5 DVK Disconnect Switches

The development board contains SPST DIP switches (S1 – S5), shown in Figure 15, placed in-line with the Pinnacle™ 100 modem I/O lines that connect to peripheral devices on the board. This functionality is provided to maximize flexibility, allowing the user to disconnect any Pinnacle™ modem I/O used by the development board, re-assign their functionality, and use them for development purposes.
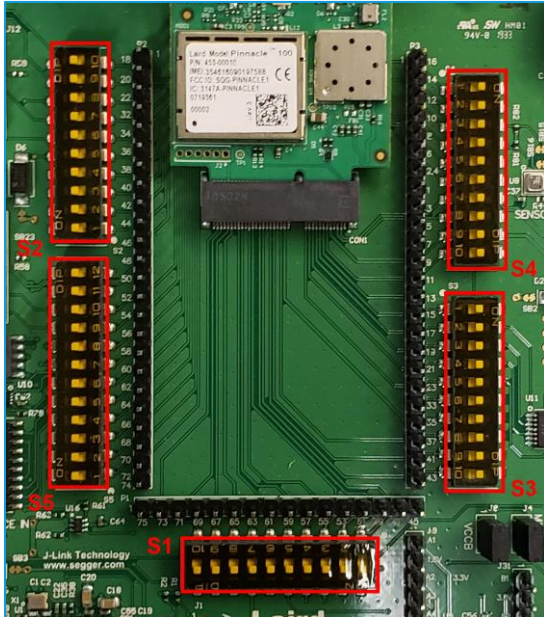

Figure 15: S1, S2, S3, S4, and S5 disconnect switches

6.6 I/O Headers Disconnect

Headers P1, P2, and P3, shown in Figure 16, are 2.54-millimeter pitch headers that provide access to the Pinnacle™ 100 modem I/O and allows for IO re-assignment when the DIP switches are open. By Default, All DIP Switches are **ON**. The silkscreen next to the header indicates the M2.#.
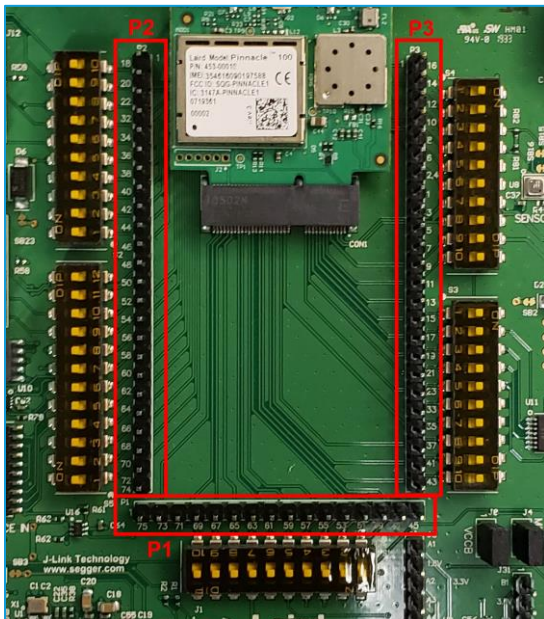

Figure 16: P1, P2, and P3 IO headers

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6.7   M2 Pins, P1 Headers, and DIP Switch Interconnection

Figure 17 shows the DVK schematic of the M2 Connector (CON1), the IO headers (P1, P2, and P3), and the DIP switches (S1, S2, S3, S4, and S5). Table 1 shows the interconnections between CON1, P1, and S1. Table 2 shows the interconnections between CON1, P2, S2, and S5. Table 3 shows the interconnections between CON1, P3, S3, and S4.

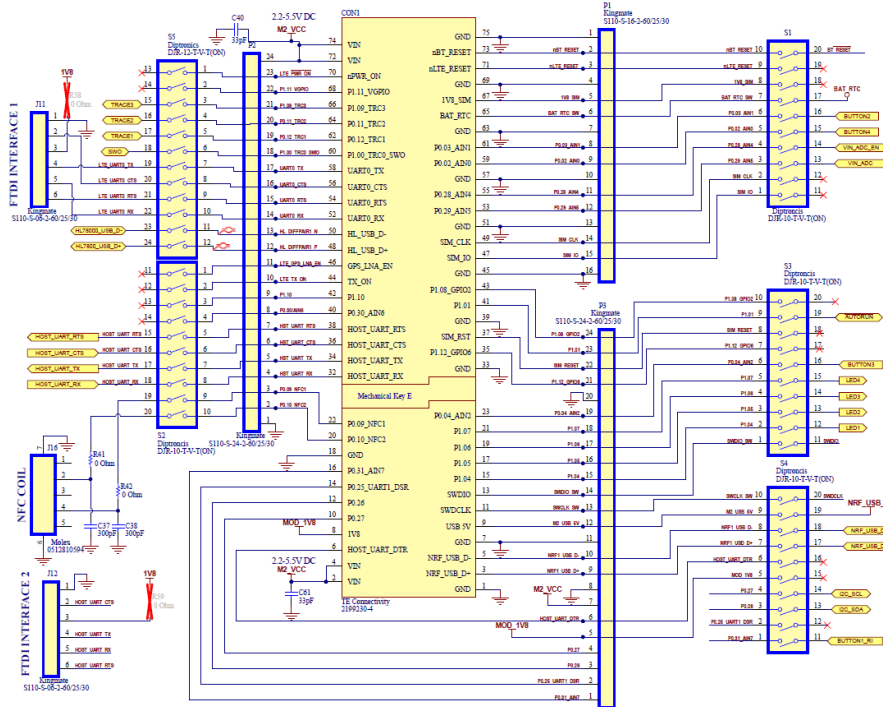**Figure 17: M2, P1, P2, P3, S1, S2, S3, S4, and S5 schematic**

Table 1: P1 and S1 signal mapping to M2 pins

Header	Position	M2.#	Net	DVK Function	Switch	Position
P1	1	75	GND			
P1	2	73	nBT_REST	SW5	S1	10
P1	3	71	nLTE_RESET		S1	9
P1	4	69	GND			
P1	5	67	1V8_SIM		S1	8
P1	6	65	BAT_RTC	CR2032 Battery	S1	7
P1	7	63	GND			
P1	8	61	P0.03_AIN1	SW2	S1	6
P1	9	59	P0.02_AIN0	SW4	S1	5
P1	10	57	GND			
P1	11	55	P0.28_AIN4	VIN_ADC_EN	S1	4
P1	12	53	P0.29_AIN5	VIN_ADC	S1	3
P1	13	51	GND			
P1	14	49	SIM_CLK		S1	2
P1	15	47	SIM_IO		S1	1
P1	16	45	GND			

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Table 2: P2, S2, and S5 signal mapping to M2 pins

Header	Position	M2.#	Net	DVK Function	Switch	Position
P2	1	18	GND			
P2	2	20	P0.10_NFC2	J16	S2	10
P2	3	22	P0.09_NFC1	J16	S2	9
P2	4	32	HOST_UART_RX	J12, FTDI USB J30	S2	8
P2	5	34	HOST_UART_TX	J12, FTDI USB J30	S2	7
P2	6	36	HOST_UART_CTS	J12, FTDI USB J30	S2	6
P2	7	38	HOST_UART_RTS	J12, FTDI USB J30	S2	5
P2	8	40	P0.30_AIN6		S2	4
P2	9	42	P1.10		S2	3
P2	10	44	TX_ON		S2	2
P2	11	46	GPS_LNA_EN		S2	1
P2	12	48	HL_USB_D+	J7 HL7800 USB	S5	12
P2	13	50	HL_USB_D-	J7 HL7800 USB	S5	11
P2	14	52	LTE_UART0_RX	J11	S5	10
P2	15	54	LTE_UART0_RTS	J11	S5	9
P2	16	56	LTE_UART0_CTS	J11	S5	8
P2	17	58	LTE_UART0_TX	J11	S5	7
P2	18	60	P1.00_TRC0_SWO		S5	6
P2	19	62	P0.12_TRC1		S5	5
P2	20	64	P0.11_TRC2		S5	4
P2	21	66	P1.09_TRC3		S5	3
P2	22	68	P1.11_VGPIO		S5	2
P2	23	70	nPWR_ON		S5	1
P2	24	72, 74	VIN			

Table 3: P3, S3, and S4 signal mapping to M2 pins

Header	Position	M2.#	Net	DVK Function	Switch	Position
P3	1	16	P0.31_AIN7	SW1	S4	1
P3	2	14	P0.25_UART1_DSR		S4	2
P3	3	12	P0.26	BME680 Sensor	S4	3
P3	4	10	P0.27	BME680 Sensor	S4	4
P3	5	8	1V8		S4	5
P3	6	6	HOST_UART_DTR		S4	6
P3	7	2, 4	VIN			
P3	8	1	GND	J10 NRF USB		
P3	9	3	NRF_USB_D+		S4	7
P3	10	5	NRF_USB_D-	J10 NRF USB	S4	8
P3	11	7	GND			
P3	12	9	USB_5V	J10 NRF USB	S4	9
P3	13	11	SWDCLK		S4	10
P3	14	13	SWDIO		S3	1

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Header	Position	M2.#	Net	DVK Function	Switch	Position
P3	15	15	P1.04	LED1 BLUE	S3	2
P3	16	17	P1.05	LED2 GREEN	S3	3
P3	17	19	P1.06	LED3 RED	S3	4
P3	18	21	P1.07	LED4 GREEN	S3	5
P3	19	23	P0.04_AIN2		S3	6
P3	20	33	GND			
P3	21	35	P1.12_GPIO6		S3	7
P3	22	37	SIM_RST		S3	8
		39	GND			
P3	23	41	P1.01		S3	9
P3	24	43	P1.08_GPIO2		S3	10

6.8 Pinnacle™ 100 UART Mapping

The 4-wire UART connections on the Pinnacle™ 100 modem and the FTDI IC are shown in Table 4. The UART connections schematic shown in Figure 18, and DVK locations shown in Figure 19.

Table 4: UART connections

Pinnacle™ 100 M2 & U5	Pinnacle™ 100 Default Function	FTDI IC UART	J12
M2.38, P0.07, U5 pin 32	HOST_UART_RTS (output)	USB_RTS	6
M2.36, P0.05, U5 pin 8)	HOST_UART_CTS (input)	USB_CTS	2
M2.34, P0.08, (U5 pin 30)	HOST_UART_TX (output)	USB_TX	4
M2.32, P0.06, (U5 pin 2)	HOST_UART_RX (input)	USB_RX	5
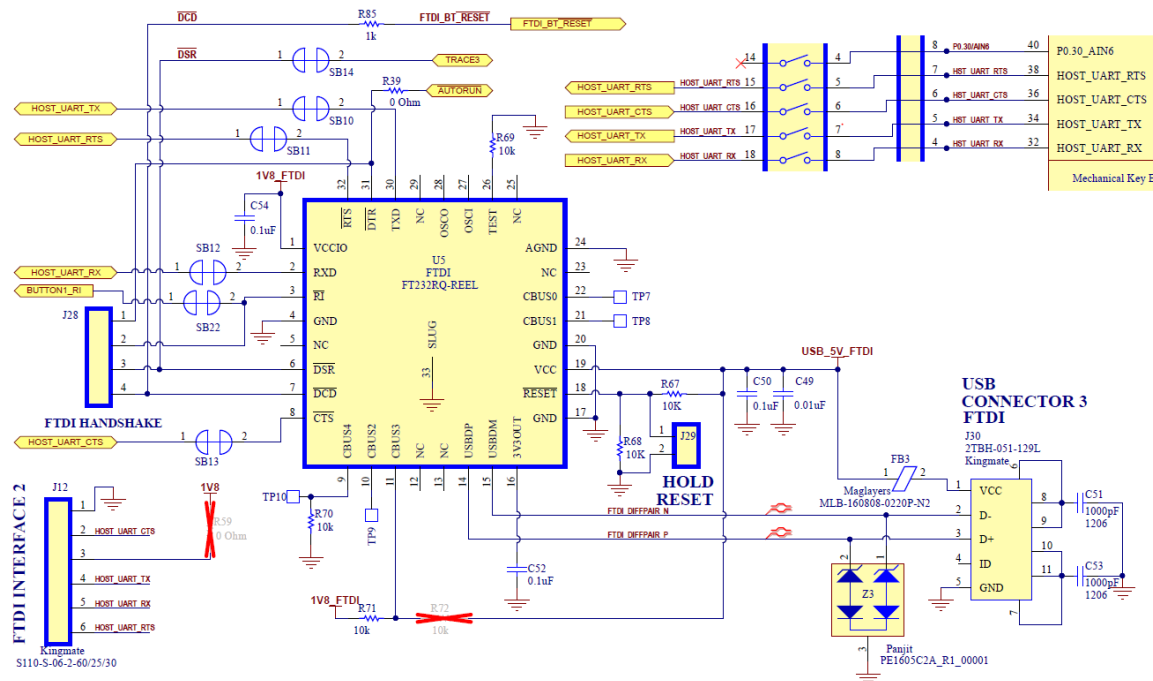
Figure 18: UART connections schematic
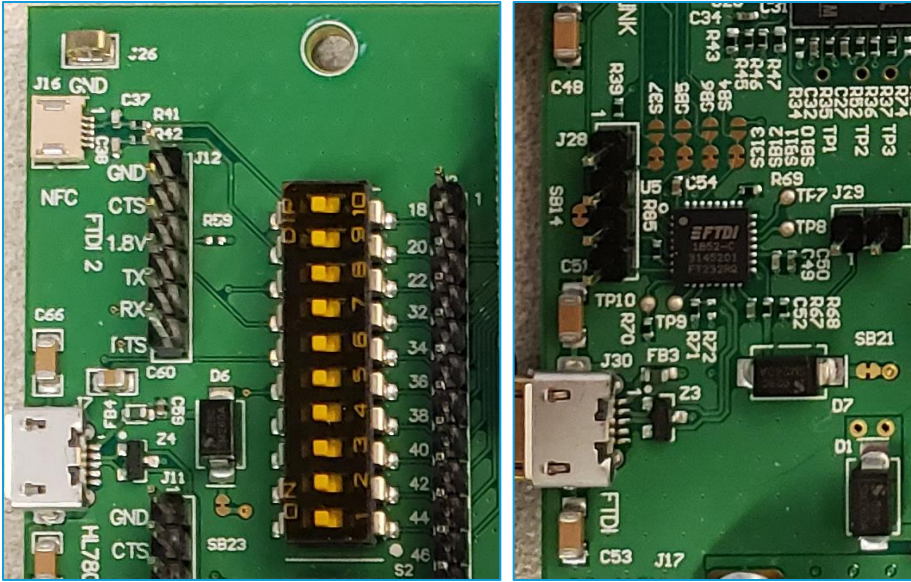
Figure 19: J30 FTDI USB and J12

6.9   Indicator LEDs

The development board includes six indicator LEDs. Four LEDs (**LED1 – LED4**) are for development use and are connected to the Pinnacle™ 100 as indicated in Table 5. The Schematic and location are shown in Figure 20.

Table 5: Pinnacle™ 100 DVK LEDs and signal mapping

Designator	Color	NRF Port Name
LED1	Blue	P1.04
LED2	Green	P1.05
LED3	Red	P1.06
LED4	Green	P1.07

Note: The Pinnacle™ 100 connections to the LEDs can be removed by switching positions 2, 3, 4, and 5 of S3 to the OFF position.

LED4 indicate the status of the bootloader.

LED5 (Red) 'ON' indicates the ATMEL SUPPLY switch is set to OFF.

LED6 (Green) 'ON' indicates Internal SWD activity.
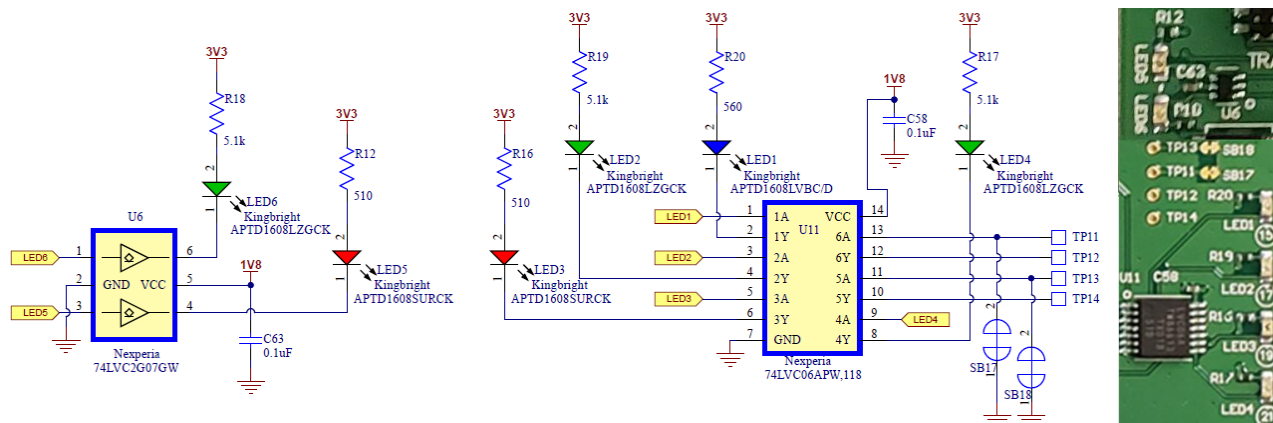
Figure 20: LEDs schematic

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6.10 Push Buttons

SW1, SW2, SW3, and SW4 are SPST-NO tact switches that when pressed provide a low logic level input to the Pinnacle™ 100 modem as indicated in Table 6. Figure 21 shows the push button schematics and DVK locations.

Table 6: Pinnacle™ 100 push button signal mapping

Designator	M2.#	NRF Port Name
SW1	M2.16	P0.31
SW2	M2.61	P0.03
SW3	M2.23	P0.04
SW4	M2.59	P0.02

Note: The Pinnacle™ 100 connections to the buttons can be removed by switching the positions of the DIP switches – S4 Position 1 (SW1), S1 Position 6 (SW2), S3 Position 6 (SW3), and S1 Position 5 (SW4) – to the OFF position.

SW1 is used by the bootloader to enter UART mode, so that must be considered if a user wants to use it for another purpose.
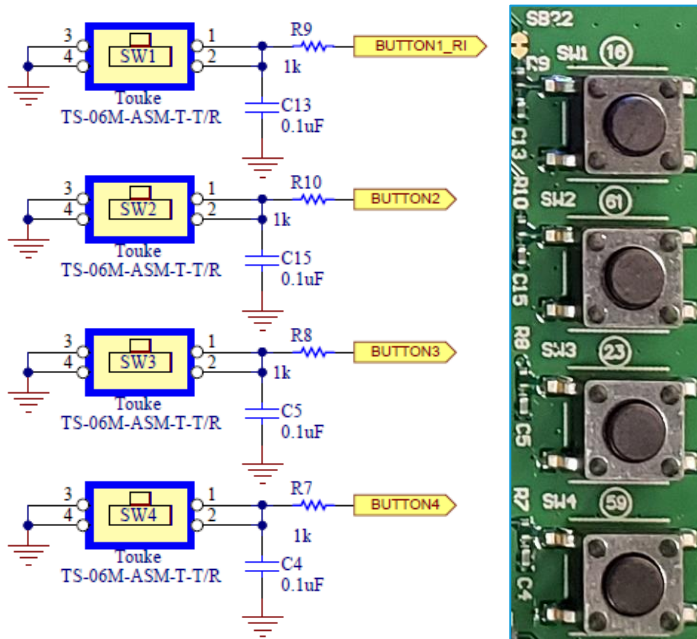
Figure 21: Push button schematic

6.11 BME680 Gas/Pressure/Temperature/Humidity Sensor

The development board includes the Bosch Sensortec BME680 air quality sensor connected to the I²C interface bus via M2.10 (SCL) and M2.11 (SDA) pins. The I²C signal traces are pulled high on the development board. Figure 22 shows the schematic and DVK location.
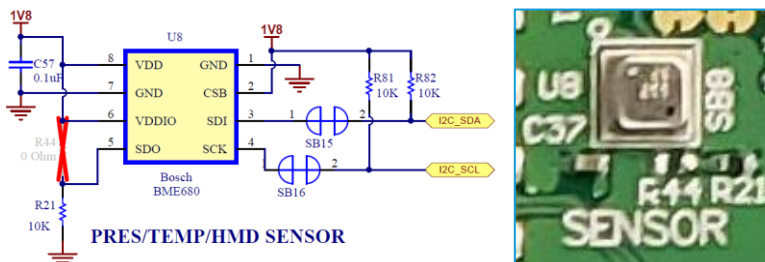
Figure 22: BEM680 sensor schematic

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6.12   VIN Monitor

The VIN to the modem can be sampled by enabling (1.8V logic) modem pin M2.55 (P0.28), VIN_ADC_EN and then taking ADC measurements using modem pin M2.53 (P0.29), shown in Figure 23.
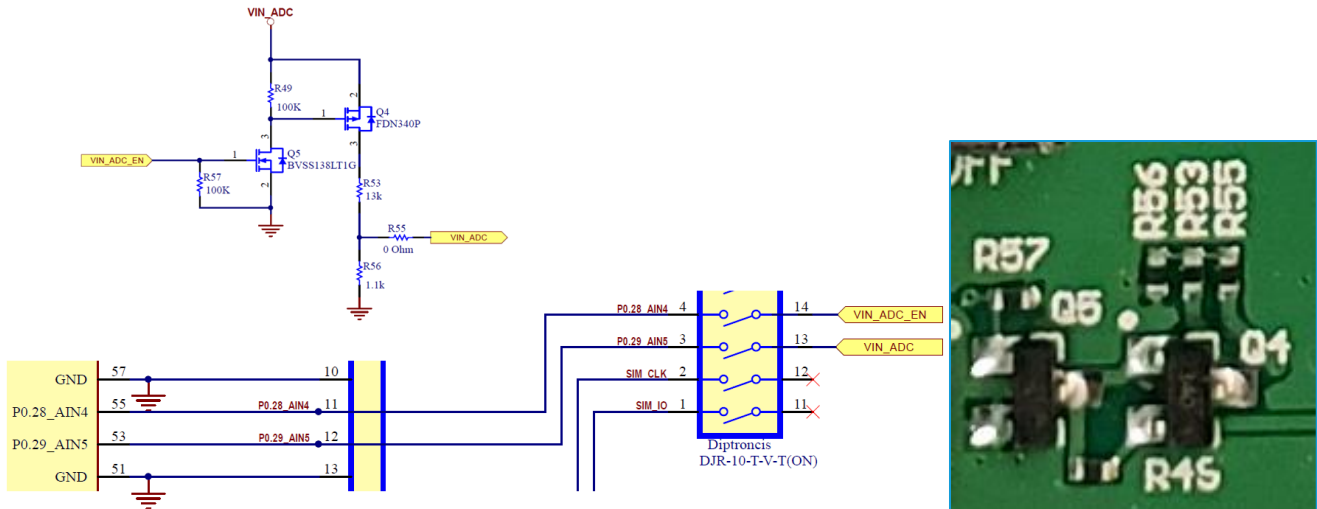
Figure 23: VIN monitor schematic

6.13   GPS Antenna

The DVK includes a GPS antenna shown in Figure 24, that is connected to the modem using J23 and a U.FL to U.FL cable.
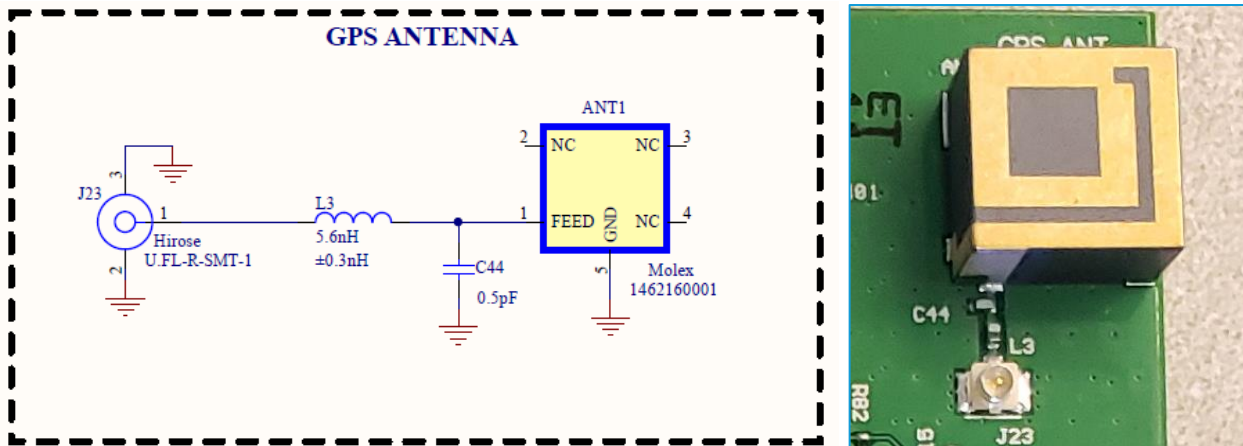

Figure 24: GPS antenna

6.14   Modem Current Consumption Measurement

Figure 25 shows a removable jumper (on J4) which is provided to break the power supply line directly to the modem, allowing the measurement of the Pinnacle™ 100 current consumption.

For normal operation, the jumper on J4 must be fitted (and is fitted by default).

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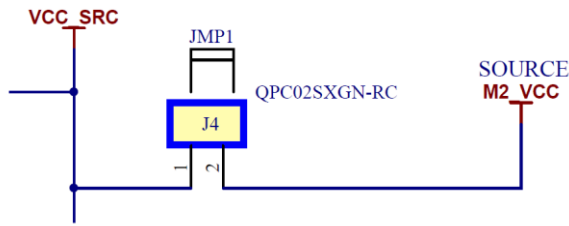
Figure 25: J4 Current measurement header

6.15 NFC External Antenna Connector and RF Matching Circuit

The NFC antenna input connector (J16) allows the Laird Connectivity supplied flex-PCB NFC antenna to be plugged in. The Pinnacle™ 100 modem NFC circuit uses two pins, M2.22 (**NFC1**) and M2.20 (**NFC2**) to connect the antenna. C37 (300pF) and C38 (300pF) are RF tuning elements for the flexi-PCB NFC antenna. Turning OFF S2 Position 9 and 10, to disconnect J16 and the RF tuning elements. Figure 26 shows the NFC schematic and location on the DVK.
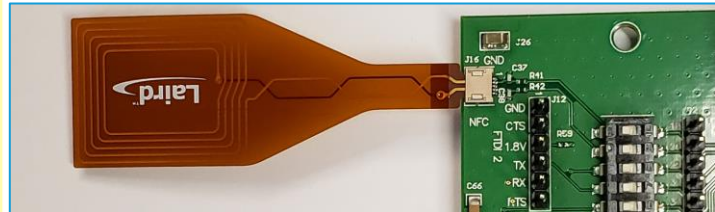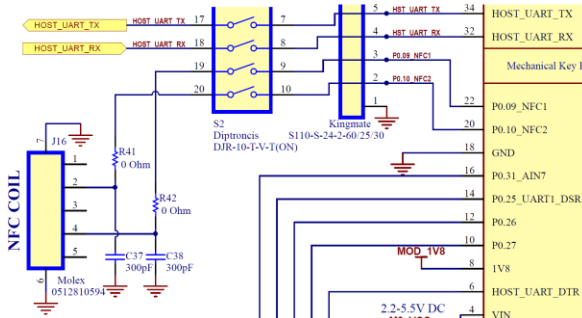
Figure 26: J16 NFC connector schematic

6.16 BAT_RTC

Placing a CR2302 battery into connector J13, shown in Figure 27, provides a backup power source to the HL7800 Real Time Clock. J13 is connected to M2.65

Figure 27: J13 BAT_RTC

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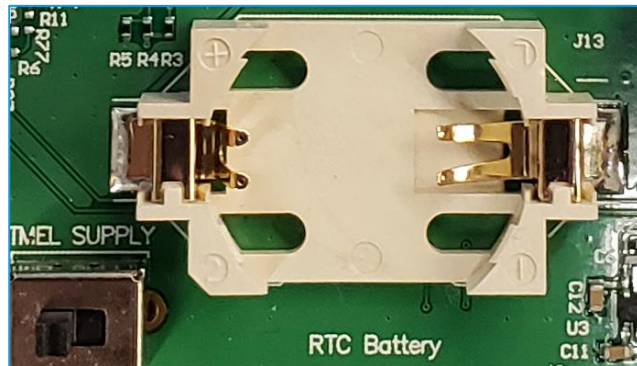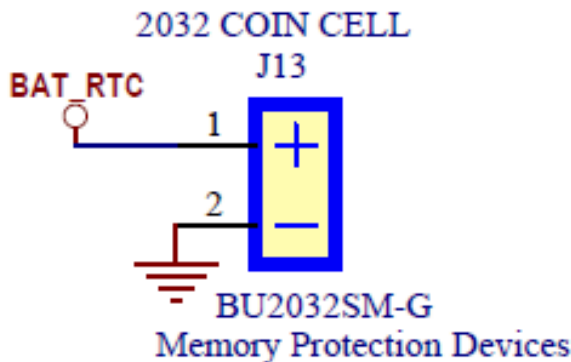
6.17 Level Shifter, U9

A 3.3V to 1.8V level shifter is available for users. J8 can be removed if a different voltage is required
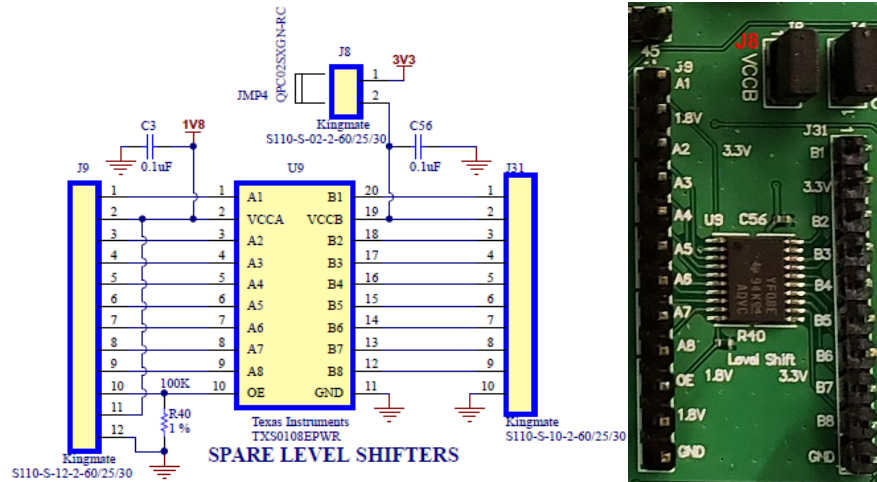
Figure 28: U9 Level Shifter

6.18 Other Features

By disconnecting DIP switches S2 # 5, 6, 7, & 8, then connecting jumpers from

J11 Pin 2 to J12 Pin 2
J11 Pin 4 to J12 Pin 4
J11 Pin 5 to J12 Pin 5
J11 Pin 6 to J12 Pin 6

The USB-UART can be connected to the HL7800 Debug port instead.

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7 SOFTWARE

The development board connects the Pinnacle™ 100 modem to a virtual COM port of a PC or other device. From a PC, you can communicate with the modem using Laird Connectivity's UwTerminalX (cross platform software available for Windows, Mac, and Linux). This utility allows connections to serial devices using any combination of the communications parameters listed in Table 7.

Table 7: UwTerminalX communication parameters for Pinnacle™ 100

Port (Windows)	1 to 255
Port (Mac/Linux)	Any /dev/tty device
Baud Rate	1200 to 1000000 **Note:** Baud rate default is 115200 for Pinnacle™ 100.
Parity	None
Data Bits	8
Stop Bits	1
Handshaking	None or CTS/RTS

Note: Baud rates higher than 115200 depend on the COM port capabilities of the host PC and may require an external USB – RS232 adapter or ExpressCard – RS232 card.

The benefits of using UwTerminalX include the following:

- Continually displayed status of DSR, CTS, DCD, and RI
- Direct control of DTR on the host PC via a check box
- Direct control of RTS, if CTS / RTS Handshaking is disabled when UWTerminalX is launched
- Sending UART BREAK signals. Following provides explanation UART Break. (https://en.wikipedia.org/wiki/Universal_asynchronous_receiver/transmitter#Break_condition)

8 ADDITIONAL DOCUMENTATION

Laird Connectivity offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the Laird Pinnacle™ 100 Product Page.

For any additional questions or queries, or to receive technical support for this Development Kit or for the Pinnacle™ 100 modem, please contact Embedded Wireless Solutions Support: https://www.lairdconnect.com/resources/support