

LC717A30UJ

Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

The LC717A30UJ is a high performance, low cost, and highly usable capacitance converter for electrostatic capacitive touch and proximity sensors.

8 capacitance-sensing input channels ideal for use in any end products that needs an array of switches. The LC717A30UJ facilitates a short system development time through its automatic calibration function and minimal external components. The detection result (ON/OFF) for each sensor is read out by the serial interface (I²C or SPI).

Features

- Differential Capacitive Detection Using Mutual Capacitance
- Operates with Small to Large Capacitance Sensor Input Pads
- Capacitance Detection Down to Femto-Farad Level
- Measurement Time 16 ms for 8 Sensors
- Minimal External Components
- Selectable Interface: I²C or SPI
- Current Consumption: 0.8 mA (V_{DD} = 5.5 V)
- Supply Voltage: 2.6 V to 5.5 V
- AEC-Q100 Qualified and PPAP Capable

Typical Applications

- Automotive: Smart Key, Control Switches, Car Audio, Proximity
- Consumer: Home Appliance, White Goods, Induction Cooking
- Industrial: Security Lock
- Computing: PC Peripherals, Audio Visual Equipment
- Lighting: Remote Control Switches

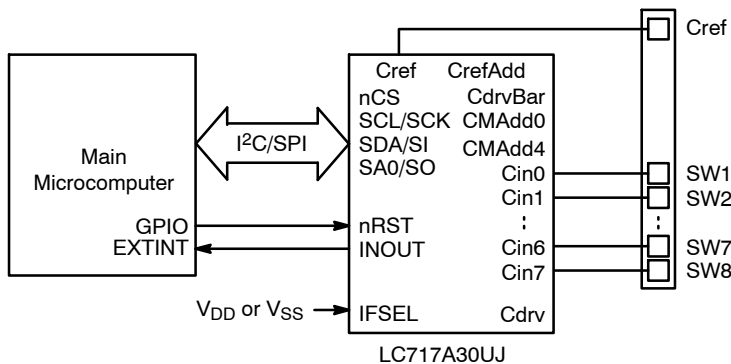
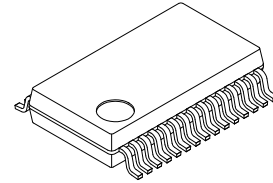


Figure 1. Application Schematic 1



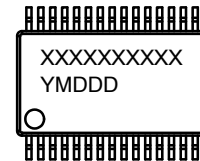
ON Semiconductor®

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SSOP30 (225 mil)
CASE 565AZ

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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8 small capacitance sensors channels and 4-wire SPI interface.

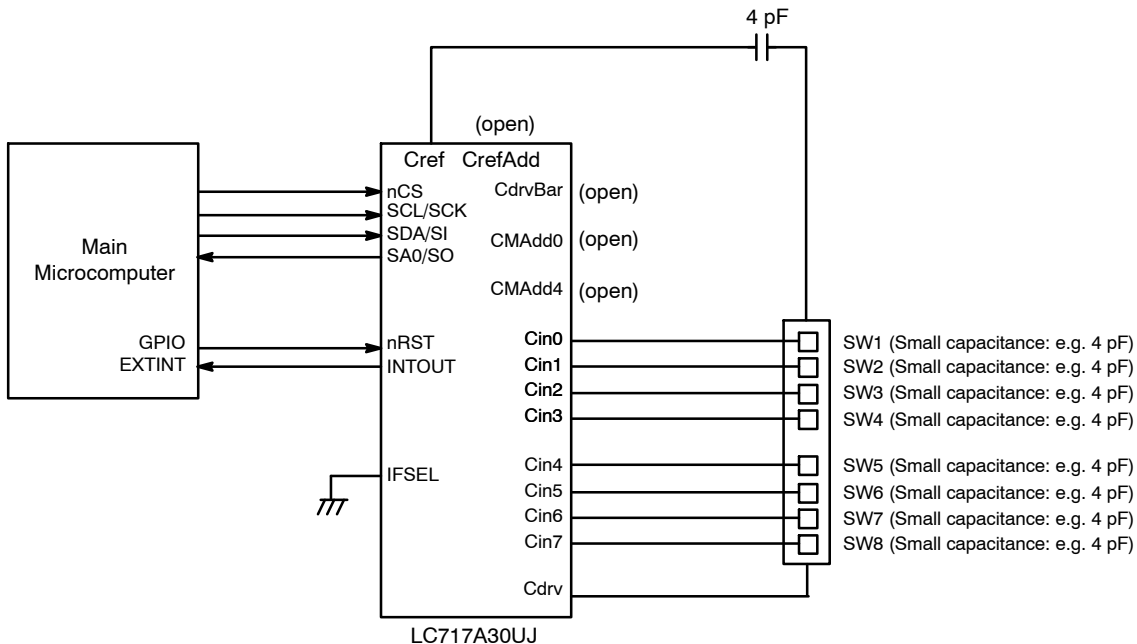


Figure 2. Application Schematic 2

8 Large capacitance sensors and I²C interface.

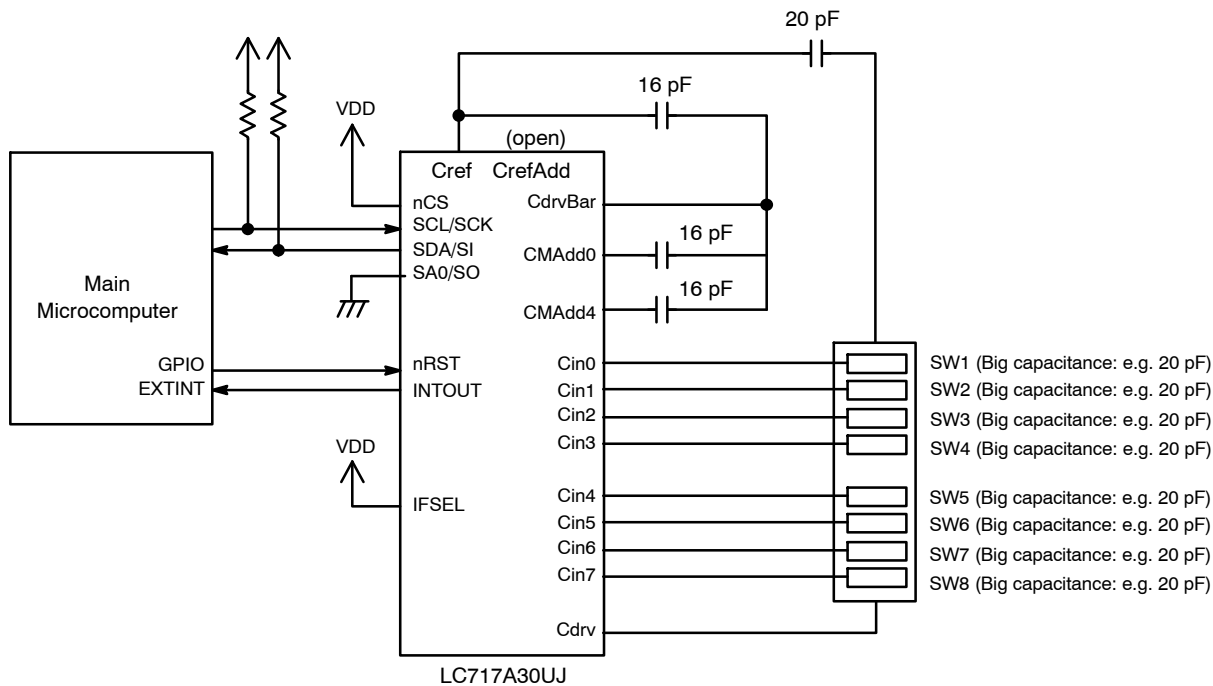


Figure 3. Application Schematic 3

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BLOCK DIAGRAM

The LC717A30UJ is a capacitance-digital converter LSI that can detect capacitance at the femto farad level. It consists a multiplexer that selects the input channels, a two-stage amplifier that detects the changes in the

capacitance and outputs analog-amplitude values, an A/D converter, a system clock, a power-on reset circuit, control logic and interface, I²C bus or SPI.

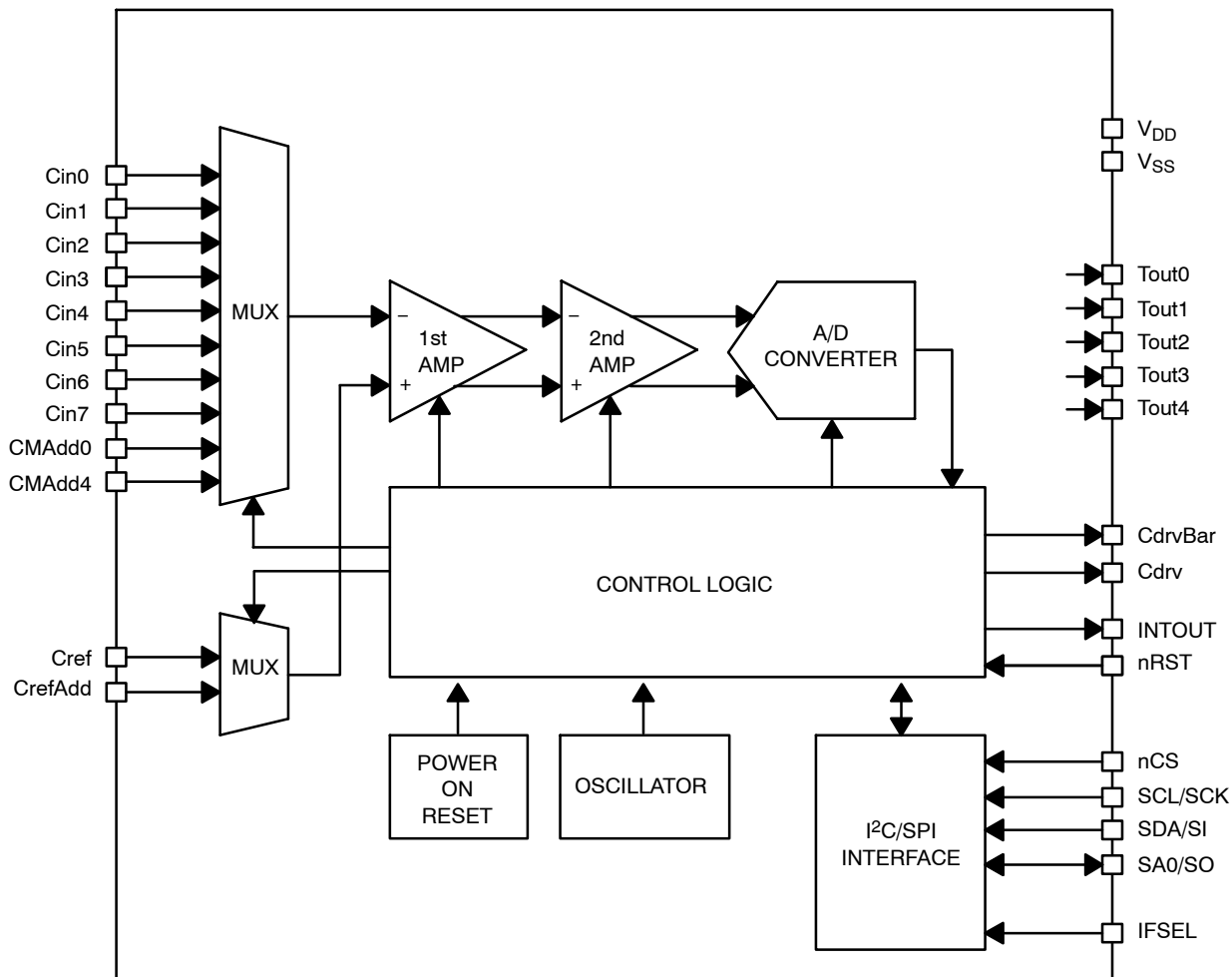


Figure 4. Simplified Block Diagram

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PIN ASSIGNMENT

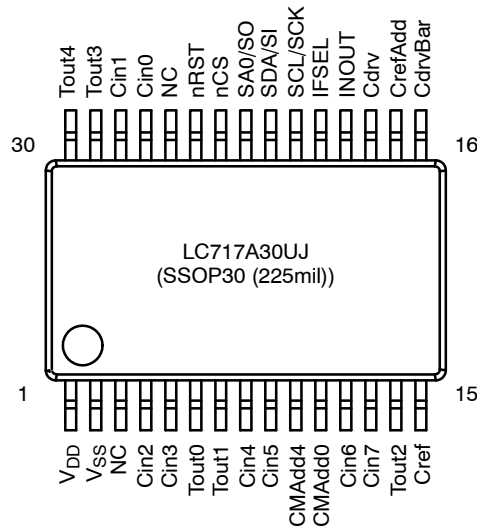


Figure 5. Pin Assignment (Top View)

Table 1. PIN ASSIGNMENT

| Pin No. | Pin Name | I/O | Description |
|---------|-----------------|-------|--|
| 1 | V _{DD} | Power | Power supply (+2.6 V to +5.5 V) (Note 1) |
| 2 | V _{SS} | Power | Ground (Notes 1, 2) |
| 3 | Non Connect | - | Connect to Ground |
| 27 | Cin0 | I/O | Sensor inputs. |
| 28 | Cin1 | I/O | Cin0 to Cin7 are connected to the inverting input of the 1st amplifier through the multiplexer. |
| 4 | Cin2 | I/O | All unused input pins must remain open. |
| 5 | Cin3 | I/O | Cdrv and Cin printed circuit board patterns should be close to each other as they are capacitively coupled. |
| 8 | Cin4 | I/O | |
| 9 | Cin5 | I/O | |
| 12 | Cin6 | I/O | |
| 13 | Cin7 | I/O | |
| 6 | Tout0 | O | Test pin, must remain open |
| 7 | Tout1 | O | Test pin, must remain open |
| 10 | CMAAdd4 | I/O | Offset capacitance input pin for the sensor inputs 4 to 7. When using large sensor pads with high capacitance, additional capacitance is added between CMAAdd4 and CdrvBar. See Figure 3. Remain open if not in use. |
| 11 | CMAAdd0 | I/O | Offset capacitance input pin for the sensor inputs 0 to 3. When using large sensor pads with high capacitance, additional capacitance is added between CMAAdd4 and CdrvBar. See Figure 3. Remain open if not in use. |
| 14 | Tout2 | O | Test pin, must remain open |
| 15 | Cref | I/O | Reference capacitance input pins. See Figures 2 and 3. |
| 17 | CrefAdd | I/O | When using large sensor pads with high capacitance, additional capacitance maybe added for Cref. See Figure 3. Remain open if not in use. |

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Table 1. PIN ASSIGNMENT (continued)

| Pin No. | Pin Name | I/O | Description |
|---------|-------------|-----|--|
| 16 | CdrvBar | O | Capacitance sensors drive signal inversion output. When using large sensor pads with high capacitance, additional capacitance is added between CMAAdd0 and CMAAdd4 and CdrvBar. See Figure 3. Remain open if not in use. |
| 18 | Cdrv | O | Capacitance sensors drive output. Cdrv and Cin printed circuit board patterns should be close to each other as they are capacitively coupled. |
| 19 | INTOUT | O | Interrupt output pin. (Active high) Remain open if not in use |
| 20 | IFSEL | I | Interface Select. IFSEL = "Low" (V_{SS}): SPI mode IFSEL = "High" (V_{DD}): I ² C mode |
| 21 | SCL/SCK | I | I ² C = SCL clock input SPI = SCK clock input |
| 22 | SDA/SI | I/O | I ² C = SDA data input/output SPI = SI data input |
| 23 | SA0/SO | I/O | I ² C = SA0 slave address selection input SPI = SO data output |
| 24 | nCS | I | I ² C = "High" (V_{DD}) SPI = nCS chip select inversion input |
| 25 | nRST | I | Reset signal inversion input pin. nRST = "Low" (V_{SS}), in reset state Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd, CdrvBar and Tout0 to Tout4 are "Hi-Z" |
| 26 | Non Connect | - | Connect to Ground |
| 29 | Tout3 | O | Test pin, must remain open |
| 30 | Tout4 | O | Test pin, must remain open |

- For noise de-coupling place a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} . The small-valued capacitor, at least 0.1 μ F, should be mounted near the LSI.
- When V_{SS} terminal is not grounded, in battery-powered mobile equipment, detection sensitivity may be degraded.

Table 2. PIN FUNCTIONS

| Pin No. | Pin Name | I/O | Pin Functions | Pin Type |
|---------|----------|-------|--|---|
| 1 | V_{DD} | Power | Power supply (+2.6 V to +5.5 V) | |
| 2 | V_{SS} | Power | Ground | |
| 27 | Cin0 | I/O | Capacitance sensor input 0 | <p>The diagram shows a circuit for a sensor input pin. The pin is connected to V_{DD} through a diode and to V_{SS} through another diode. A resistor R is connected between the pin and a node. This node is also connected to a buffer and an amplifier (AMP).</p> |
| 28 | Cin1 | I/O | Capacitance sensor input 1 | |
| 4 | Cin2 | I/O | Capacitance sensor input 2 | |
| 5 | Cin3 | I/O | Capacitance sensor input 3 | |
| 8 | Cin4 | I/O | Capacitance sensor input 4 | |
| 9 | Cin5 | I/O | Capacitance sensor input 5 | |
| 12 | Cin6 | I/O | Capacitance sensor input 6 | |
| 13 | Cin7 | I/O | Capacitance sensor input 7 | |
| 10 | CMAAdd4 | I/O | Additional offset capacitance input pin for the sensor inputs 4 to 7 | |
| 11 | CMAAdd0 | I/O | Additional offset capacitance input pin for the sensor inputs 0 to 3 | |
| 15 | Cref | I/O | Reference capacitance input | |
| 17 | CrefAdd | I/O | Additional Reference capacitance input | |

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Table 2. PIN FUNCTIONS (continued)

| Pin No. | Pin Name | I/O | Pin Functions | Pin Type |
|---------|----------|-----|--|----------|
| 6 | Tout0 | O | Output for tests | |
| 7 | Tout1 | O | Output for tests | |
| 14 | Tout2 | O | Output for tests | |
| 29 | Tout3 | O | Output for tests | |
| 30 | Tout4 | O | Output for tests | |
| 16 | CdrvBar | O | Capacitance sensors drive signal inversion output | |
| 18 | Cdrv | O | Capacitance sensors drive output | |
| 19 | INTOUT | O | Interrupt output | |
| 20 | IFSEL | I | Switching control input of the serial data communication interface | |
| 21 | SCL/SCK | I | SCL clock input (I ² C) | |
| | | I | SCK clock input (SPI) | |
| 24 | nCS | I | nCS chip select inversion input (SPI) | |
| 25 | nRST | I | External reset signal inversion input | |
| 22 | SDA/SI | I/O | SDA data input/output (I ² C) | |
| | | I | SI data input (SPI) | |
| 23 | SA0/SO | I | SA0 slave address selection input (I ² C) | |
| | | O | SO data output (SPI) | |

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ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V, T_A = +25°C)

| Symbol | Parameter | Value | Unit |
|-------------------|--|------------------------------|------|
| V _{DD} | Supply Voltage Range | -0.3 to +6.5 | V |
| V _{IN} | Input Voltage Range (Note 3) | -0.3 to V _{DD} +0.3 | V |
| V _{OUT} | Output Voltage Range (Note 4) | -0.3 to V _{DD} +0.3 | V |
| I _{OP} | Peak Output Current Range (Notes 4, 5) | -8.0 to +8.0 | mA |
| I _{OA} | Total Outputs Current Range (Note 6) | -40 to +40 | mA |
| P _{dmax} | Maximum Power Dissipation (Note 7) | 160 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Apply to Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd, SCL/SCK, SDA/SI, SA0, nCS, nRST, IFSEL.
- Apply to Cdrv, CdrvBar, SDA, SO, INTOUT, Tout0 to Tout4.
- Total value with duty cycle under 25%.
- Limited to one pin, with duty cycle under 50%.
- T_A = 105°C, Single-layer glass epoxy board (76.1 × 114.3 × 1.6 mm).

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V)

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---|---------------------|---------------------|------|
| V _{DD} | Operating Supply Voltage Range (Note 8) | 2.6 | 5.5 | V |
| V _{IH} | Input High-level Voltage Range (Note 9) | 0.8 V _{DD} | V _{DD} | V |
| V _{IL} | Input Low-level Voltage Range (Note 9) | 0 | 0.2 V _{DD} | V |
| T _A | Ambient Temperature Range | -40 | 105 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- For noise de-coupling place a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS}. The small-valued capacitor, at least 0.1 μF, should be mounted near the LSI. In addition, it is recommended that the power supply ripple + noise is less than ±40 mV.
- Apply to SCL/SCK, SDA/SI, SA0, nCS, nRST, IFSEL.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.6 to 5.5 V, V_{SS} = 0 V, T_A = -40 to + 105°C, Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 121 kHz.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------------|--|--|---------------------|------|---------------------|------|
| COMMON | | | | | | |
| V _{OH1} | Output High-level Voltage (Note 10) | I _O = -1.5 mA, V _{DD} = 2.6 to 3.6 V | 0.8 V _{DD} | - | - | V |
| V _{OH2} | | I _O = -3.0 mA, V _{DD} = 3.6 to 5.5 V | 0.8 V _{DD} | - | - | V |
| V _{OL1} | Output Low-level Voltage (Note 10) | I _O = +1.5 mA, V _{DD} = 2.6 to 3.6 V | - | - | 0.2 V _{DD} | V |
| V _{OL2} | | I _O = +3.0 mA, V _{DD} = 3.6 to 5.5 V | - | - | 0.2 V _{DD} | V |
| V _{OL3} | Tout0 to Tout4 pins Output Low-level Voltage | I _O = +1.5 mA | - | - | 0.2 V _{DD} | V |
| V _{OL4} | SDA pin Output Low-level Voltage | I _O = +3.0 mA | - | - | 0.4 | V |
| I _{IH} | Input High-level Current (Note 11) | V _I = V _{DD} | - | - | 1.0 | μA |
| I _{IL} | Input Low-level Current (Note 11) | V _I = V _{SS} | -1.0 | - | - | μA |
| I _{OFF} | Output Off Leakage Current (Note 12) | V _I = V _{DD} or V _I = V _{SS} | -1.0 | - | 1.0 | μA |
| I _{DD1} | Current Consumption | Initial setting, Long interval operation, Sensor pins are open (Note 13), V _{DD} = 5.5 V | - | 0.8 | 2.2 | mA |
| I _{DD2} | | Initial setting, Short interval operation, Sensor pins are open (Note 13), V _{DD} = 5.5 V | - | 3.25 | 6.5 | mA |
| I _{STBY} | | Sleep mode (Sleep period) Sensor pins are open (Note 13) | - | 0.1 | 70 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.6$ to 5.5 V, $V_{SS} = 0$ V, $T_A = -40$ to $+105^\circ\text{C}$, Unless otherwise specified, the Cdrv drive frequency is $f_{CDRV} = 121$ kHz.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
|--------|-----------|-----------|-----|-----|-----|------|

CAPACITANCE SENSOR FUNCTION

| | | | | | | |
|---------------|--------------------------------------|---|--------|----------|-----------|--------|
| $C_{inSENSE}$ | Cin Detection Sensitivity | Measurements conducted using the test mode in the LSI, Minimum gain setting | 0.0476 | 0.068 | 0.0884 | LSB/FF |
| I_{Cin} | Sensor Pin Leakage Current (Note 14) | $V_I = V_{DD}$ or $V_I = V_{SS}$ | – | ± 25 | ± 500 | nA |
| f_{CDRV} | Cdrv Drive Frequency | With 121 kHz setting | 84.85 | 121.21 | 157.57 | kHz |

POWER-ON RESET FUNCTION

| | | | | | | |
|-------------|--|-----------------|-----|---|-----|---------------|
| t_{NRST} | nRST Minimum Pulse Width | | 1.0 | – | – | μs |
| t_{POR} | Power-on Reset Time | | – | – | 20 | ms |
| t_{POROP} | Power-on Reset Operation Condition: Hold Time | | 10 | – | – | ms |
| V_{POROP} | Power-on Reset Operation Condition: Input Voltage | | – | – | 0.1 | V |
| t_{VDD} | Power-on Reset Operation Condition: Power Supply Rise Rate | 0 V to V_{DD} | 1.0 | – | – | V/ms |

INTERVAL OPERATION TIMING

| | | | | | | |
|--------------|---------------------|---|-----|-----|-----|----|
| T_{LIVAL1} | Long Interval Time | $V_{DD} = 2.6$ to 4.5 V, Long interval mode (Long interval time is set to 101 ms) | 35 | 101 | 145 | ms |
| T_{LIVAL2} | | $V_{DD} = 4.5$ to 5.5 V, Long interval mode (Long interval time is set to 101 ms) | 40 | 101 | 125 | ms |
| T_{SIVAL1} | Short Interval Time | $V_{DD} = 2.6$ to 4.5 V, Short interval mode (Short interval time is set to 5 ms) | 1.7 | 5 | 7.3 | ms |
| T_{SIVAL2} | | $V_{DD} = 4.5$ to 5.5 V, Short interval mode (Short interval time is set to 5 ms) | 1.9 | 5 | 6.3 | ms |

I²C COMPATIBLE BUS INTERFACE TIMING

| | | | | | | |
|---------------|-------------------------------------|----------|-----|---|-----|---------------|
| f_{SCL} | SCL Clock Frequency | SCL | – | – | 400 | kHz |
| $t_{HD; STA}$ | START Condition Hold Time | SCL, SDA | 0.6 | – | – | μs |
| t_{LOW} | SCL Clock Low Period | SCL | 1.3 | – | – | μs |
| t_{HIGH} | SCL Clock High Period | SCL | 0.6 | – | – | μs |
| $t_{SU; STA}$ | Repeated START Condition Setup Time | SCL, SDA | 0.6 | – | – | μs |
| $t_{HD; DAT}$ | Data Hold Time | SCL, SDA | 0 | – | 0.9 | μs |
| $t_{SU; DAT}$ | Data Setup Time | SCL, SDA | 0.5 | – | – | μs |
| t_r/t_f | SDA, SCL Rise/Fall Time | SCL, SDA | – | – | 0.3 | μs |
| $t_{SU; STO}$ | STOP Condition Setup Time | SCL, SDA | 0.6 | – | – | μs |
| t_{BUF} | STOP-to-START Bus Release Time | SCL, SDA | 2.5 | – | – | μs |

SPI INTERFACE TIMING

| | | | | | | |
|---------------|-----------------------------|--------------|-----|---|-----|-----|
| f_{SCK} | SCK Clock Frequency | SCK | – | – | 5.0 | MHz |
| t_{LOW} | SCK Clock Low Time | SCK | 100 | – | – | ns |
| t_{HIGH} | SCK Clock High Time | SCK | 100 | – | – | ns |
| t_r/t_f | Input Signal Rise/Fall Time | nCS, SCK, SI | – | – | 300 | ns |
| $t_{SU; NCS}$ | nCS Setup Time | nCS, SCK | 200 | – | – | ns |
| $t_{SU; SCK}$ | SCK Clock Setup Time | nCS, SCK | 100 | – | – | ns |
| $t_{SU; SI}$ | Data Setup Time | SCK, SI | 100 | – | – | ns |
| $t_{HD; SI}$ | Data Hold Time | SCK, SI | 100 | – | – | ns |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.6$ to 5.5 V, $V_{SS} = 0$ V, $T_A = -40$ to $+105^\circ\text{C}$, Unless otherwise specified, the Cdrv drive frequency is $f_{CDRV} = 121$ kHz.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
|--------|-----------|-----------|-----|-----|-----|------|

SPI INTERFACE TIMING

| | | | | | | |
|--------------|--|----------|-----|---|-----|----|
| $t_{HD;NCS}$ | nCS Hold Time | nCS, SCK | 200 | – | – | ns |
| $t_{HD;SCK}$ | SCK Clock Hold Time | nCS, SCK | 700 | – | – | ns |
| t_{CPH} | nCS Standby Pulse Width | nCS | 300 | – | – | ns |
| t_{CHZ} | Output High Impedance Time from nCS | nCS, SO | – | – | 100 | ns |
| t_V | Output Data Determination Time | SCK, SO | – | – | 100 | ns |
| $t_{HD;SO}$ | Output Data Hold Time | SCK, SO | 0 | – | – | ns |
| t_{CLZ} | Output Low Impedance Time from SCK Clock | SCK, SO | 100 | – | – | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Apply to Cdrv, CdrvBar, SO, INTOUT.

11. Apply to SCL/SCK, SDA/SI, SA0, nCS, nRST, IFSEL.

12. Apply to Cdrv, CdrvBar, SDA, SO.

13. Sensor pins (Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd) are open condition.

14. Apply to Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd.

Table 3. ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) [†] |
|---------------|--|---------------------------------------|
| LC717A30UJ-AH | SSOP30 (225 mil) (Pb-Free / Halogen Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FUNCTIONAL DESCRIPTION

Power-on Reset (POR)

When power is turned on, power-on reset is enabled, it is released after power-on reset time, t_{POR} . Power-on reset operation condition; Power supply rise rate t_{VDD} must be at least 1.0 V/ms.

Since INTOUT pin changes from “High” to “Low” at the same time as reset release, it is possible to verify the timing of release of reset externally. During power-on reset, Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd, and CdrvBar are unknown.

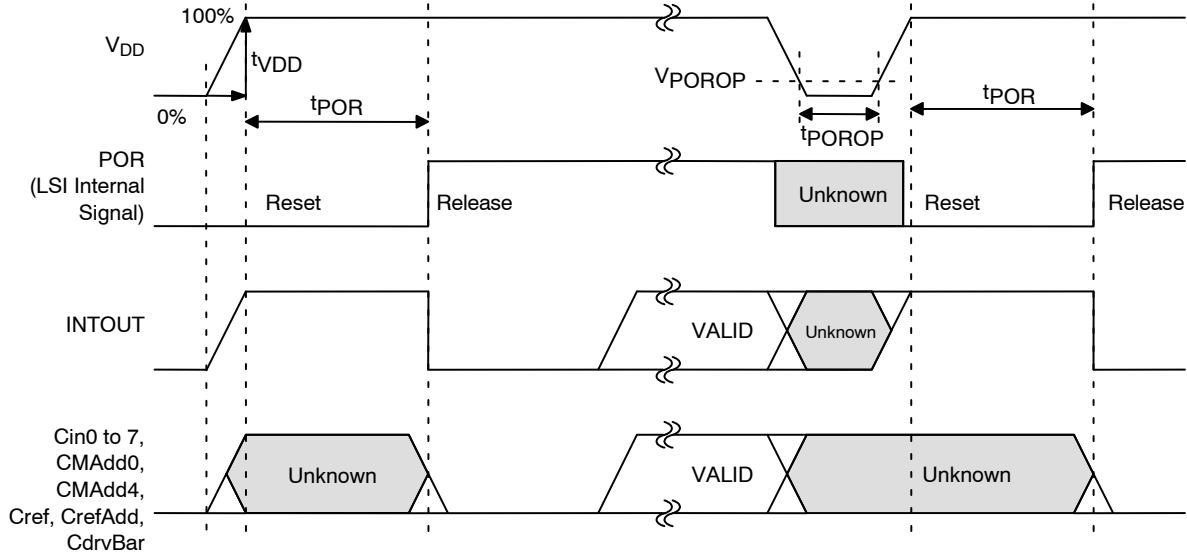


Figure 6. Power-on Sequence by the Power-on Reset

External Reset (nRST)

Reset State nRST = “Low”. Pins Cin0 to Cin7, CMAAdd0, CMAAdd4, Cref, CrefAdd and CdrvBar, are “Hi-Z” during reset state. The reset state is released after t_{POR} .

Since INTOUT pin changes from “High” to “Low” at the same time as the released of reset, it is possible to verify the timing of release of reset externally.

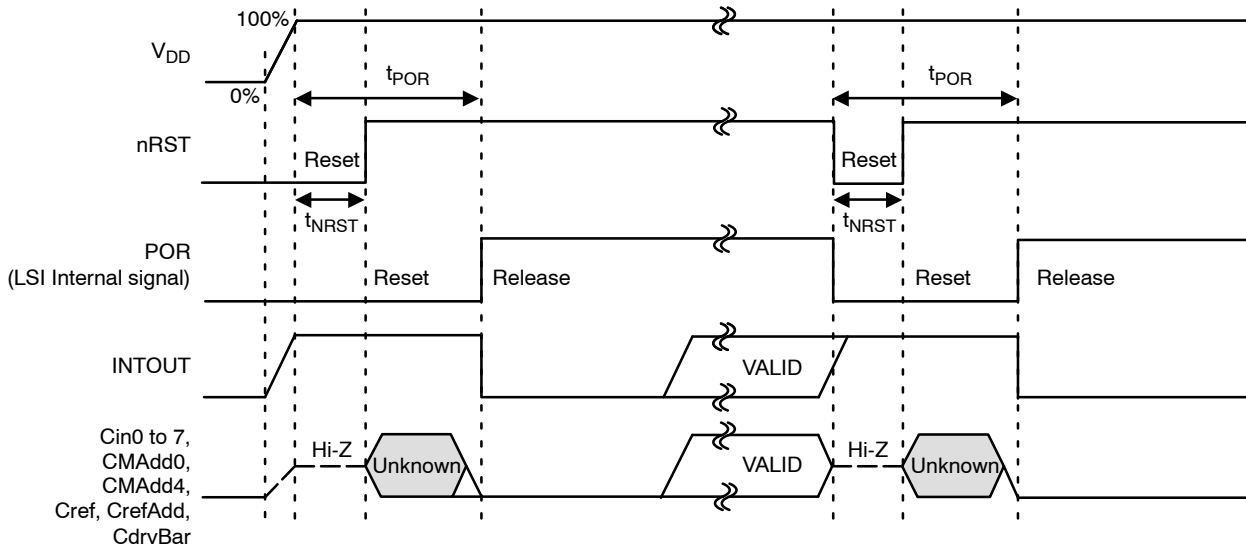


Figure 7. Power-on Sequence by the External Reset

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I²C Data Timing

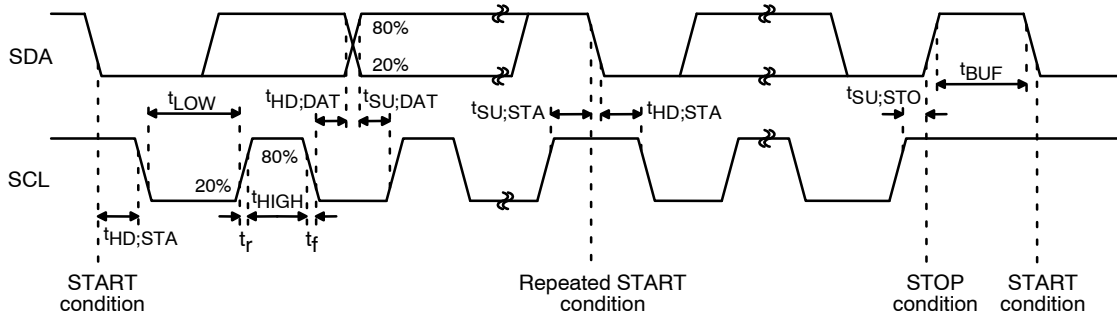


Figure 8. I²C Data Timing

I²C Communication Formats

Write Format

When using the Write format of I²C the data can be written into sequentially incremented addresses.



Figure 9. I²C Write Format

Read Format

When using the Read format of I²C the data can be read from sequentially incremented addresses.

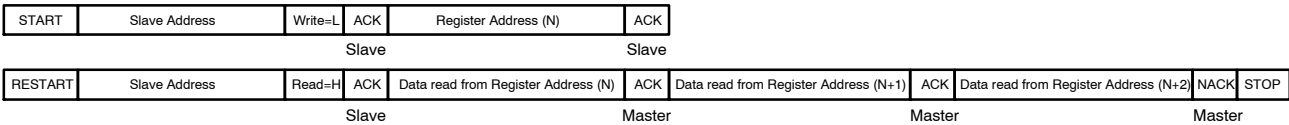


Figure 10. I²C Read Format

I²C Slave Address

SA0 pin is used to select the slave address

Table 4. I²C SLAVE ADDRESS

| SA0 Pin Input | 7 bit Slave Address | Binary Notation | 8 bit Slave Address |
|---------------|---------------------|-------------------|---------------------|
| Low | 0x16 | 00101100b (Write) | 0x2C |
| | | 00101101b (Read) | 0x2D |
| High | 0x17 | 00101110b (Write) | 0x2E |
| | | 00101111b (Read) | 0x2F |

SPI Data Timing (Mode 0/Mode 3)

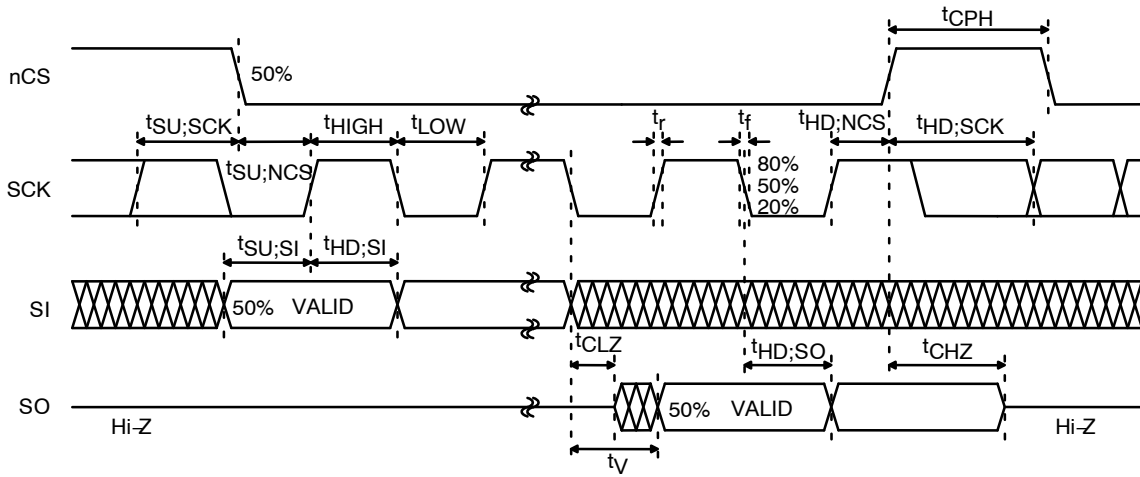


Figure 11. SPI Data Timing

SPI Write Format (Example of Mode 0)

When using the SPI Write format the data can be written into sequentially incremented addresses with preserving nCS = "L".

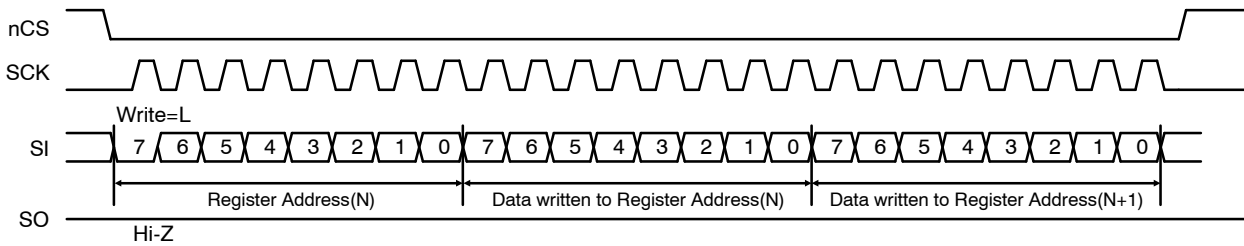


Figure 12. SPI Write Format

SPI Read Format

When using the SPI Read format the data can be read from sequentially incremented addresses with preserving nCS = "L".

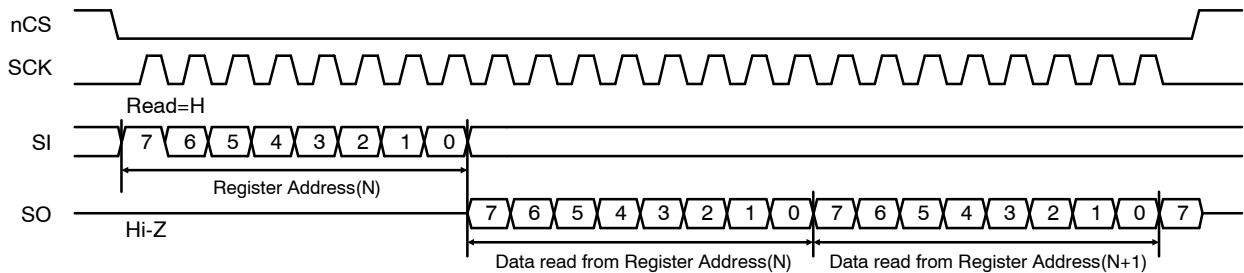


Figure 13. SPI Read Format

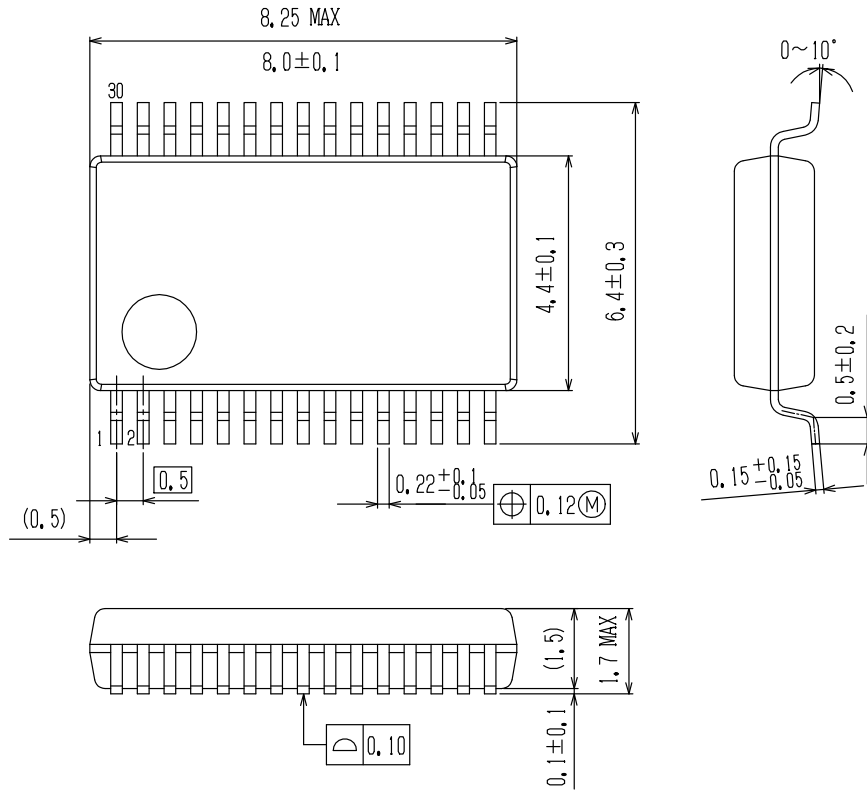
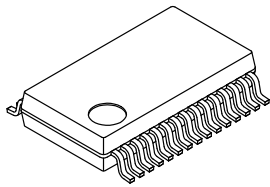
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

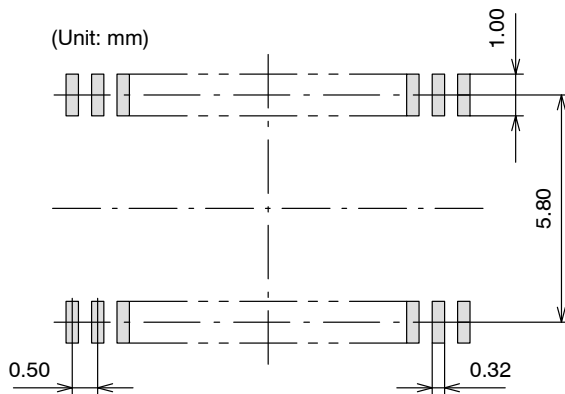


SSOP30 (225 mil)
CASE 565AZ
ISSUE A

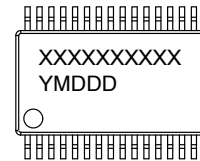
DATE 25 OCT 2013



SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 Y = Year
 M = Month
 DDD = Additional Traceability Data

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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