Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDL5V0B12P1Q0 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

TESDL5V0B12P1Q0 is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDL5V0B12P1Q0 may be used to provide ESD protection up to ±30kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 6A (8/20μs) according to IEC61000-4-5.

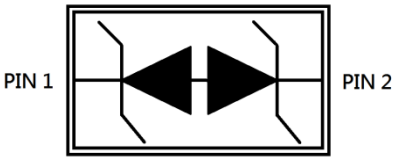
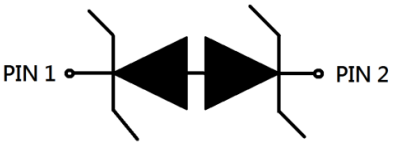
FEATURES

- ESD protect for 1 line with bidirectional
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC61000-4-5 (Lightning) 6A (8/20μs)
- Suitable for 5V and below, operating voltage applications
- Ultra small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- Computers and peripherals
- Portable devices
- Network communication devices
- Notebooks and servers

Pb-Free RoHS COMPLIANT HALOGEN FREE

PACKAGE: DFN0603-2L	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Peak pulse power (tp = 8/20μs)	P_{PK}	70	W
Peak pulse current (tp = 8/20μs)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Junction temperature	T_J	125	°C
Operating temperature range	T_{OP}	-40 to +85	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	5.1	-	-	V
Reverse leakage current	V_{RWM} = 5V, T_J = 25°C	I_R	-	-	1	μA
Clamping voltage(1)	I_{PP} = 1A, tp = 8/20μs	V_C	-	-	8	V
	I_{PP} = 6A, tp = 8/20μs		-	-	12	V
Clamping voltage(2)	I_{TLP} = 16A, tp = 100ns	V_{CL}	-	14.2	-	V
Junction capacitance	f = 1MHz, V_R = 0V	C_J	-	9	12	pF
Dynamic resistance(2)		R_{DYN}	-	0.38	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. RDYN is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDL5V0B12P1Q0 M7G	DFN0603-2L	10,000 / 7" Tape & Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

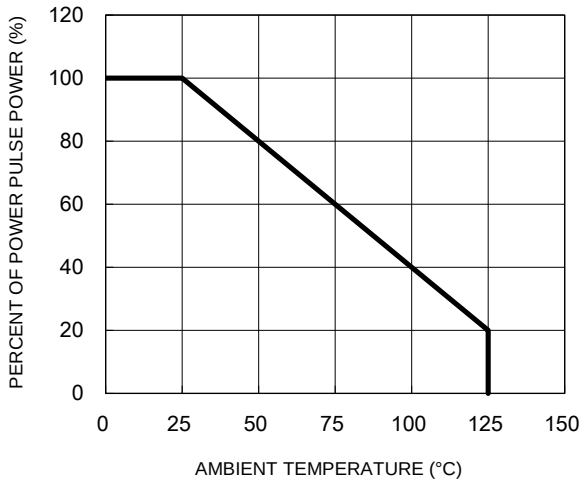


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

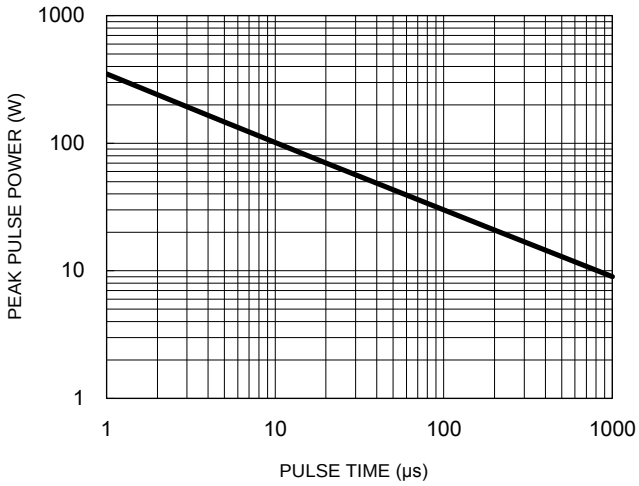


Fig.3 Clamping Voltage vs. Peak Pulse Current

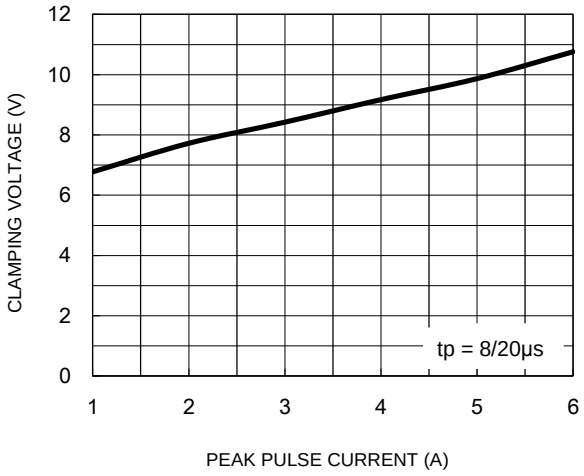


Fig.4 Capacitance vs. Reverse Voltage

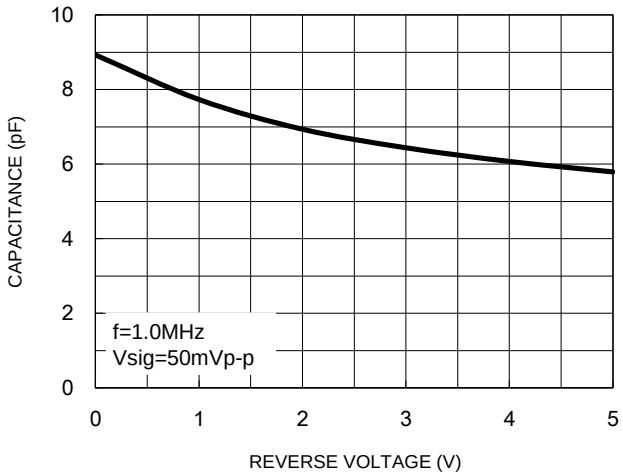
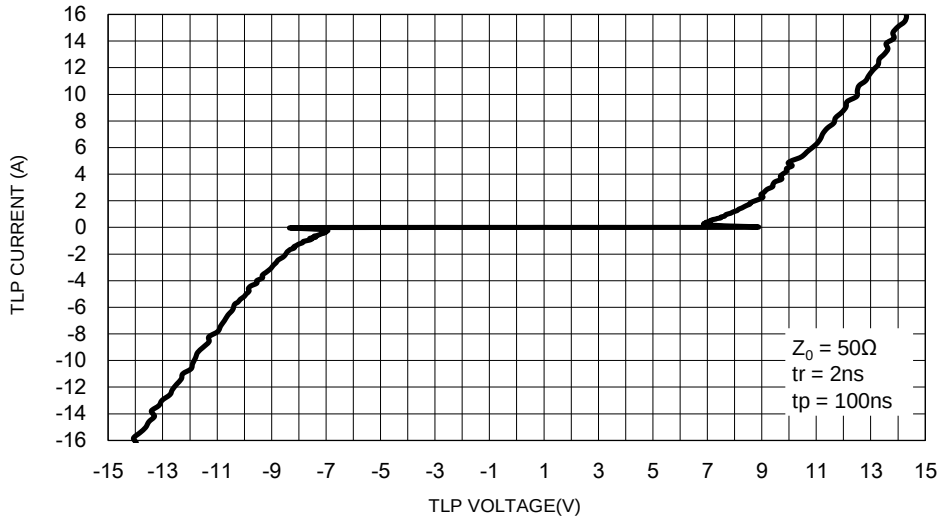


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform per IEC61000-4-5

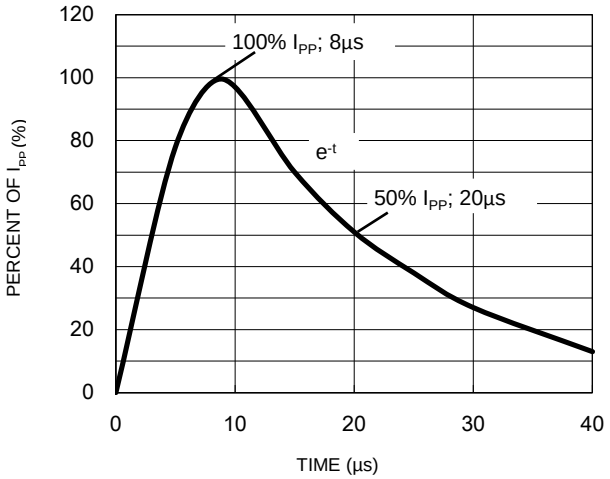
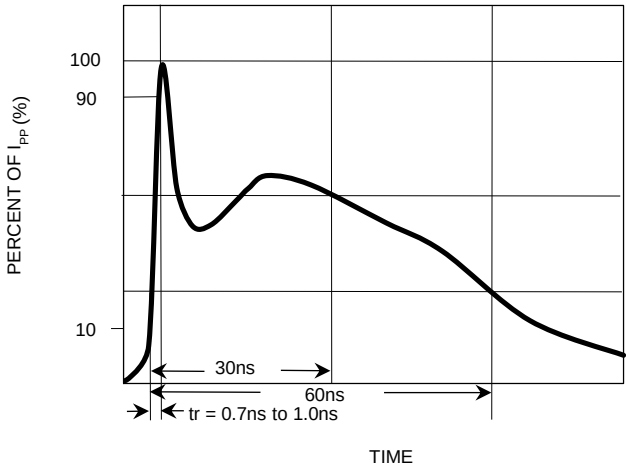


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

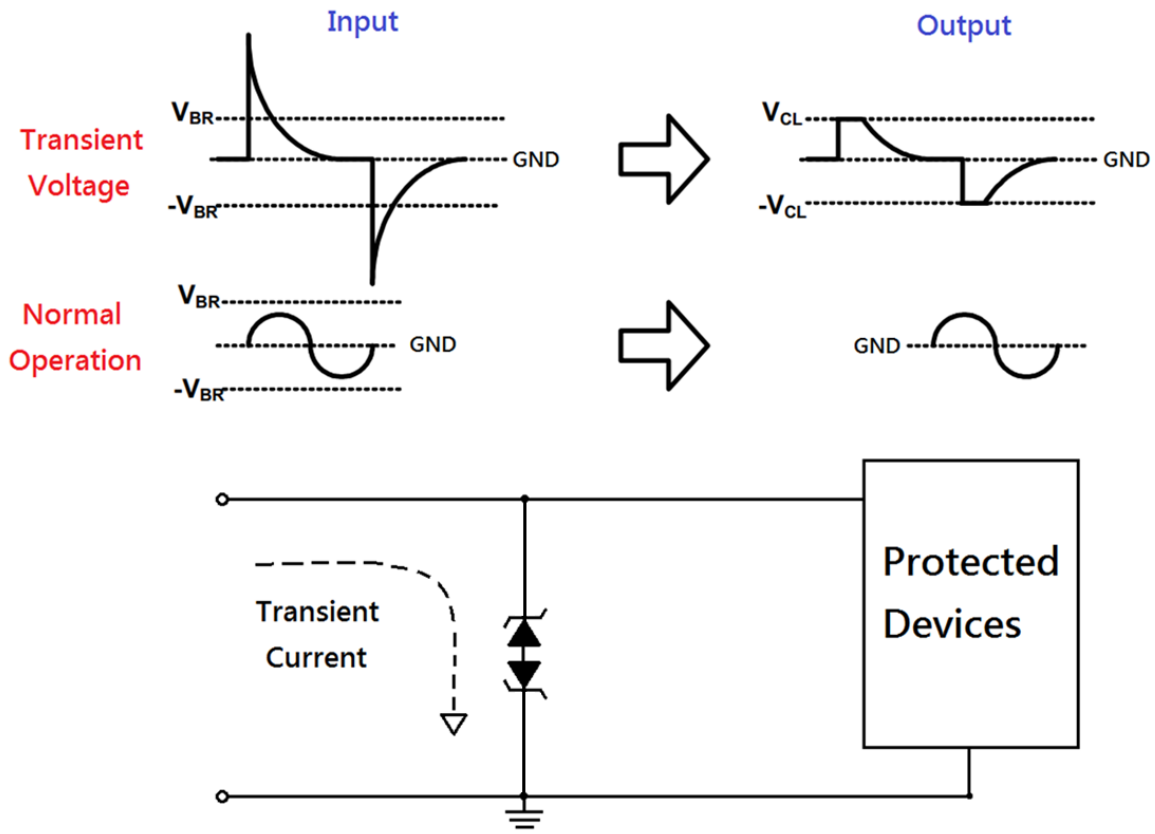
Device Connection

The TESDL5V0B12P1Q0 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.
The usage of the TESDL5V0B12P1Q0 is shown in Fig1.Protected line, such as data line, control line, or power line. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDL5V0B12P1Q0 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

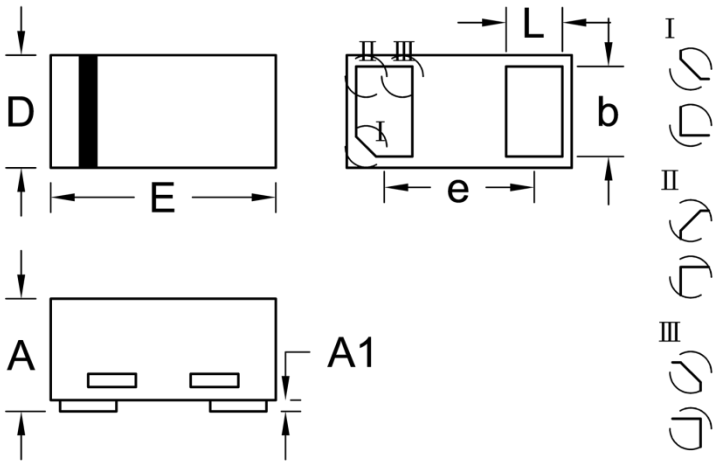
- Let the path length between the protected lines and the TESDL5V0B12P1Q0 minimize.
- Place the TESDL5V0B12P1Q0 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

Fig.1 ESD protection by TESDL5V0B12P1Q0



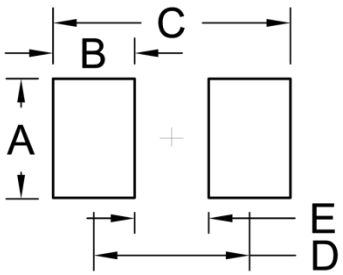
PACKAGE OUTLINE DIMENSIONS

DFN0603-2L



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	0.23	0.34	0.009	0.013
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
D	0.25	0.37	0.010	0.015
E	0.55	0.67	0.022	0.026
e	0.40		0.016	
L	0.10	0.20	0.004	0.008

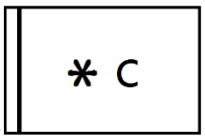
SUGGESTED PAD LAYOUT



Symbol	Unit (mm)	Unit (inch)
A	0.32	0.013
B	0.22	0.009
C	0.64	0.025
D	0.42	0.017
E	0.20	0.008

Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

MARKING DIAGRAM



* = Month Code

C = Device Code

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